PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN APMS/25/15690

Analog, Power, MEMS & Sensors (APMS)

ST Manufacturing Reshaping (Analog_EWS ONLY CTA to TPY): Qualification of TPY (Singapore) as new EWS Location.

Issue date: 3rd November 2026

Description of the change

Following Corporate PCI 15383 (Early Notification), about Company reshaping program, please be informed that EWS (Electrical Wafer Sorting) of Analog products listed here below will be transferred from ST Catania (Italy) to ST Singapore.

Change Summary:

	Former	New
EWS/Location	ST Catania	ST Singapore

Traceability:

Internal Traceability – Date code-
Step tracked in ST production systems and available real time on demand

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Affected products

Refer to below table for involved Commercial Products.
Specific devices not expressly listed in this table are included in this change.

CP code involved in qualification			
VBG08H-E	VN9008AJTR	VND7006DAYTR-E	VNH7100AS-E
VBG08HTR-E	VN9008LAJTR	VND7E025AJ	VNH7100BASTR
VN01TTTR	VN9012AJTR	VND7E025AJTD1	VNH7110ASTR
VN5D05TR-E	VN9012LAJTR	VND7E025AJTR	VNH9013GY
VN5D10TR-E	VN9016AJ	VND7E040AJ	VNH9013GYTR
VN5E006ASPTR-E	VN9016AJTR	VND7E040AJTR	VNH9013YTR
VN5E050JTR-E	VN9016LAJTR	VND7E050AJTD1	VNH9030AQ
VN5E160MSTR-E	VN9D5D20F	VND7E050AJTR	VNH9030AQTR
VN5HV16AH-E	VN9D5D20FTR	VND7E070AJ	VNHD7008AYTR
VN5HV16AHTR-E	VN9D7D20F	VND7E070AJTR	VNHD7012AYTR
VN5T006ASPTR-E	VN9D7D20FTR	VND9008AJ	VNJ6TD1
VN5T016AHTR-E	VN9E30F	VND9008AJTR	VNQ5E250AJTR-E
VN7004DAY	VN9E30FTR	VND9008LAJTR	VNQ6004SATR-E
VN7004DAY-E	VN9Q25D70F	VND9012AJTR	VNQ6040STR-E
VN7004DAYTR	VN9Q25D70FTR	VND9012LAJTR	VNQ7024DAY
VN7004DAYTR-E	VND5E004ATR-E	VND9016AJ	VNQ7024DAY-E
VN7004SLHTR	VND5HV100AJ-E	VND9016AJTR	VNQ7024DAYTR
VN7007AHTR	VND5HV100AJTR-E	VND9016LAJTR	VNQ7024DAYTR-E
VN7007ALH-E	VND5T035AKTR-E	VND9025AJ	VNQ7E100AJ
VN7007ALHTR	VND5T035LAKTR-E	VND9025AJTR	VNQ7E100AJTR
VN7008AJTR	VND5T050AKTR-E	VNF9D5F	VNQ7E110AJ
VN750PSTR-E	VND5T100AJTR-E	VNF9D5FTR	VNQ7E110AJTR
VN7E010AJTR	VND5T100LAJTR-E	VNF9Q20F	VNQ9025AJ
VN9004AJTR	VND7004AYTR	VNF9Q20FTR	VNQ9025AJTR
VN9006AJ	VND7006DAY	VNH3SP30TR-E	VNQ9050LAJ
VN9006AJTR	VND7006DAY-E	VNH7070AY	VNQ9050LAJTR
VN9006LAJTR	VND7006DAYTR	VNH7070AYTR	VNQ9080AJTR

Dual die (one of the dice qualified)
Qualification on going
Qualified

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Reason

Die manufacturing: ST manufacturing reshaping program - Corporate PCI - Early Notification.

Date of implementation

First shipments forecast: one month after Qualification completion date (see below qualification results date for reference).

Impact of change	
Form	Not Impacted
Fit	Not Impacted
Function	Not Impacted
Reliability	Not Impacted
Processibility	Not Impacted

Qualification of the change (plan)

Qualification will be performed according to ST guidelines and ZVEI (ID SEM-TF01) for Automotive products.

		Compliant with ST internal spec and ZVEI Guideline Product and Process Changes (PCN) 5.0 (Automotive products)		
		Line readiness	ED (Electrical Distribution, Cpk, analysis *)	Parametric analysis (Yield, Bin to Bin *)
Product		•	•	•

* Comparing wafers in old vs. new location

Disposition of former products

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Delivery of current products will be done until stock depletion.

Qualification results

Qualification report including qualification results is enclosed at the end of this document:

Qualification completion date: Mar-2026.

Sampling plan

Customer samples are not planned; the switch of production will occur at product validation.

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Qualification Report

Transfer of EWS (Electrical Wafer Sorting) from ST Catania (Italy) to ST Singapore for Analog products

General Information	
Commercial Product	See above list
Product perimeter	Analog
Product group	APMS
Maturity level	Qualified

Locations	
Diffusion Plant	Multiple
Assembly Plant	Multiple
Reliability Lab	N/A

Assessment	
Pass	X
Fail	

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1. APPLICABLE AND REFERENCE DOCUMENTS

ZVEI	Change Standard Methodology

2. GLOSSARY

EWS	Electrical Wafer Sorting

3. RELIABILITY EVALUATION OVERVIEW

3.1. Objective

The objective of this report is to qualify the transfer of EWS (Electrical Wafer Sorting) from ST Catania (Italy) to ST Singapore for products detailed in PCN: Qualification plan conducted following ZVEI matrix as follow:

	ZVEI DEFAULT	ZVEI WITH CONDITIONS	ST SELECTED	REASON FOR EXCEPTION OF TESTS
AEC-Q101 Revision E	•	•	X	
Parametric Verification	•	•	X	No characterization planned as only EWS is transferred*
Parameter-Analysis: Comparison of current with changed device characterization, electrical distribution	•	•	X	

*Characterization is meant for Final Test transfer, not applicable for this EWS transfer

3.2. Conclusion

Qualification Plan requirements have been fulfilled without exception. Line readiness tests, Electrical Distribution, Cpk, Yield and Bin to Bin analysis and comparison have all shown positive results.
Based on these results, all devices are ready for the EWS transfer from ST Catania to ST Singapore.

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4. PRODUCT OR TEST VEHICLE CHARACTERISTICS

4.1. Device description

Refer to ST specification:

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4.2. Construction note

	All parts listed in page 6
Wafer/Die fab. information	
Wafer fab manufacturing location	multiple
Technology	multiple
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore

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5. TEST RESULTS SUMMARY

5.1. Lot information

Lot #	Part Number	Comment
Lot 1	VN5D10TR-E	
Lot 2 - 11	VNQ7024DAYTR	Dual die product Lot 2 (die 1) / lot 11 (die 2)
Lot 3	VND9012AJTR	
Lot 4	VND9012LAJTR	
Lot 5	VNHD7012AYTR	Note 1: partial result, one die evaluated on two dice to be evaluated (multicide package)
Lot 6	VND7E025AJTR	
Lot 7	VNQ7E100AJTR	
Lot 8	VN9004AJTR	
Lot 9	VN9012AJTR	
Lot 10	VN9012LAJTR	
Lot 12	VNF9D5F	
Lot 13	VNHD7008AYTR	
Lot 14	VNH7110ASTR	
Lot 15	VND9008AJTR	
Lot 16	VN7E010AJTR	
Lot 17	VN9D7D20F	
Lot 18	VNQ9025AJ	
Lot 19	VN5T006ASPTR-E	
Lot 20	VND7E070AJ	
Lot 21	VND5T035AKTR-E	
Lot 22	VND7004AYTR	
Lot 23	VND7004AYTR	
Lot 24	VNQ5E250AJTR-E	
Lot 25	VNQ5E250AJTR-E	
Lot26	VNJ6TD1	
Lot 27	VNF9Q20F	
Lot 28	VND5HV100AJ-E	
Lot 29	VND5T100LAJTR-E	
Lot 30	VN9D5D20F	
Lot 31	VN5D05TR-E	
Lot 32	VND7006DAY	
Lot 33	VND7006DAYTR	
Lot 34	VN5E050JTR-E	

Detailed results in below chapter will refer to these references.

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5.2. Test plan

Qualification of the change (plan)

Qualification will be performed according to and ST guidelines and ZVEI (ID SEM-TF01) for Automotive products.

	Compliant with ST internal spec and ZVEI Guideline Product and Process Changes (PCN) 5.0 (Automotive products)		
	Line readiness	ED (Electrical Distribution, Cpk, analysis *)	Parametric analysis (Yield, Bin to Bin *)
Product	•	•	•

*comparing wafers in ol vs. new location

5.3. results summary

Item	Qualification activity	Sample size	VN5D10TR-E	VNQ7024DAYTR (die 1)	VND9012AJTR	VND9012LAJTR	VNHD7012AYTR (Note 1)	VND7E025AJTR	VNQ7E100AJTR	VN9004AJTR	VN9012AJTR	VN9012LAJTR
	Line readiness	1 lot	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	ED (Electrical Distribition, Cpk analysis)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

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EWS line transfer	Parametric analysis (Yield, Bin to Bin)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Item	Qualification activity	Sample size	VNQ7024DAYTR (die 2)	VNF9D5F	VNHD7008AYTR	VNH7110ASTR	VND9008AJTR	VN7E010AJTR	VN9D7D20F	VNQ9025AJ	VN5T006ASPTR-E
EWS line transfer	Line readiness	1 lot	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	ED (Electrical Distribition, Cpk analysis)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	Parametric analysis (Yield, Bin to Bin)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

Item	Qualification activity	Sample size	VND7E070AJ	VND5T035AKTR-E	VND7004AYTR	VND7004AYTR	VNQ5E250AJTR-E	VNQ5E250AJTR-E	VNJ6TD1	VNF9Q20F	VND5HV100AJ-E
EWS line transfer	Line readiness	1 lot	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	ED (Electrical Distribition, Cpk analysis)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
	Parametric analysis (Yield, Bin to Bin)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

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Item	Qualification activity	Sample size	VND5T100LAJTR-E	VN9D5D20F	VN5D05TR-E	VND7006DAY	VND7006DAYTR	VN5E050JTR-E
EWS line transfer	Line readiness	1 lot	PASS	PASS	PASS	PASS	PASS	PASS
	ED (Electrical Distribition, Cpk analysis)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS
	Parametric analysis (Yield, Bin to Bin)	1 full wafers	PASS	PASS	PASS	PASS	PASS	PASS

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