Product Change Notification: SYST-23FTKA341

Date:

29-Oct-2026

Product Category:

N-Channel Enhancement Mode Mosfets

Notification Subject:

Data Sheet - N-Channel Enhancement-Mode Vertical DMOS FET

Affected CPNs:

SYST-23FTKA341_Affected_CPN_10292026.pdf
SYST-23FTKA341_Affected_CPN_10292026.csv

Notification Text:

SYST-23FTKA341
Microchip has released a new Datasheet for the N-Channel Enhancement-Mode Vertical DMOS FET of devices. If you are using one of these devices please read the document located at **N-Channel Enhancement-Mode Vertical DMOS FET**. **Notification Status:** Final **Description of Change:** • Updated Pin Function Table to accurately describe the device. • Updated drawings in Section 5.0 “Packaging Information”. **Impacts to Data Sheet:** None **Impacts to Data Sheet:** None **Change Implementation Status:** Complete **Date Document Changes Effective:** 29 Oct 2026 **NOTE:** Please be advised that this is a change to the document only the product has not been changed. **Markings to Distinguish Revised from Unrevised Devices:** N/A

Attachments:

N-Channel Enhancement-Mode Vertical DMOS FET

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Affected Catalog Part Numbers (CPN)

VN2110NW

VN2110NW-D614

VN2110K1-G

VN2110ND

VN2110ND-D491

VN2110ND-ADO

VN2110NW-8

VN2110NW-D614-8

VN2110NW-8AD1

VN2110

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low CISS and Fast Switching Speeds
- High Input Impedance and High Gain

Applications

- Motor Controls
- Converters
- Amplifiers
- Switches
- Power Supply Circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

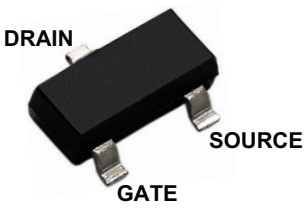
General Description

The VN2110 low-threshold, Enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited for a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Type

3-lead SOT-23
(Top view)



See Table 3-1 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Gate-to-Source Voltage..... ±20V
Operating Ambient Temperature, T_A ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	V_{GS} = 0V, I_D = 1 mA
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	2.4	V	V_{GS} = V_{DS}, I_D = 1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	–3.8	–5.5	mV/°C	V_{GS} = V_{DS}, I_D = 1 mA (**Note 1**)
Gate Body Leakage Current	I_{GSS}	—	0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	100	µA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 1**)
On-State Drain Current	$I_{D(ON)}$	0.6	—	—	A	V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	4.5	6	Ω	V_{GS} = 5V, I_D = 75 mA
		—	3	4	Ω	V_{GS} = 10V, I_D = 500 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta_{RDS(ON)}$	—	0.7	1	%/°C	V_{GS} = 10V, I_D = 500 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All AC parameters are not 100% sample tested.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Forward Transconductance	G_{FS}	150	400	—	mmho	V_{DS} = 25V, I_D = 500 mA
Input Capacitance	C_{ISS}	—	35	50	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common-Source Output Capacitance	C_{OSS}	—	13	25	pF	
Reverse Transfer Capacitance	C_{RSS}	—	4	5	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	3	5	ns	V_{DD} = 25V, I_D = 600 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	5	8	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	6	9	ns	
Fall Time	t_f	—	5	8	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	1.2	1.8	V	V_{GS} = 0V, I_{SD} = 600 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	400	—	ns	V_{GS} = 0V, I_{SD} = 600 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 µs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	θ_{JA}	—	203	—	°C/W	

THERMAL CHARACTERISTICS

Package	**I_D (Note 1) (Continuous) (mA)**	**I_D (Pulsed) (mA)**	**Power Dissipation at T_A = 25°C (W)**	**I_{DR} (Note 1) (mA)**	**I_{DRM} (mA)**
3-lead SOT-23	200	800	0.36	200	800

Note 1: I_D (continuous) is limited by maximum T_J.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

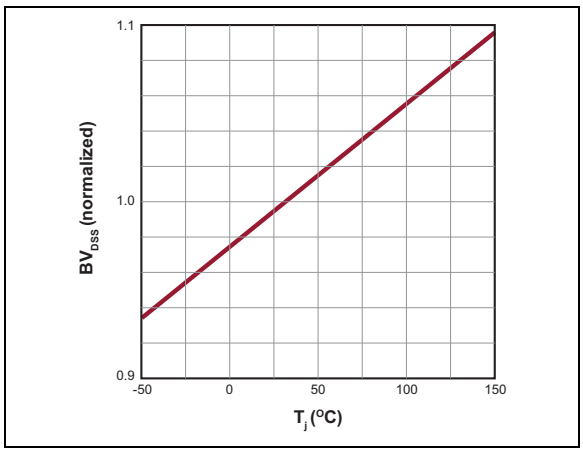


FIGURE 2-1: *BV_{DSS} Variation with Temperature.*

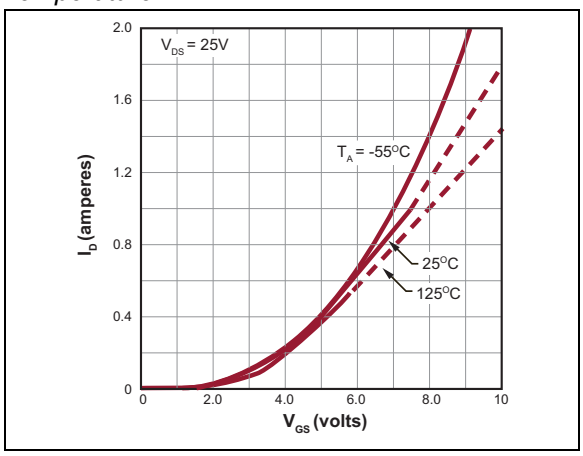


FIGURE 2-2: *Transfer Characteristics.*

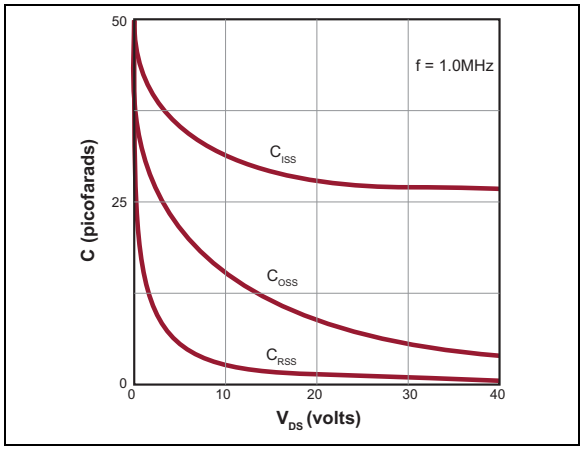


FIGURE 2-3: *Capacitance vs. Drain-to-Source Voltage.*

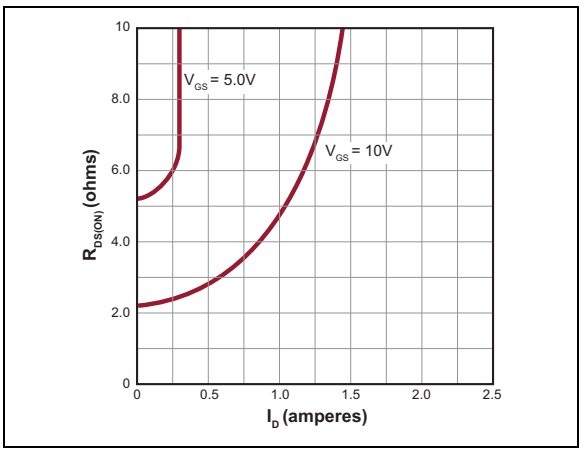


FIGURE 2-4: *On-Resistance vs. Drain Current.*

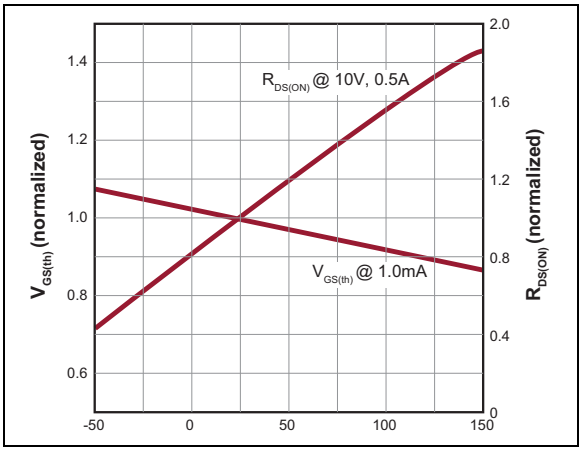


FIGURE 2-5: *$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature.*

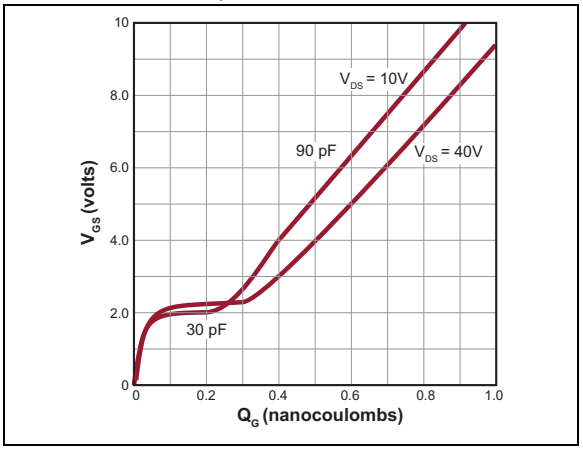


FIGURE 2-6: *Gate Drive Dynamic Characteristics.*

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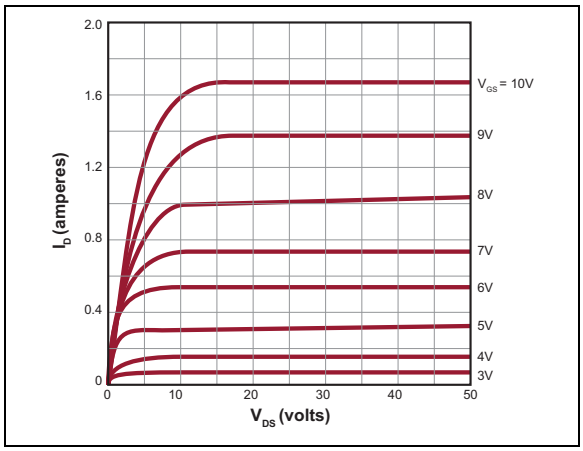


FIGURE 2-7: *Output Characteristics.*

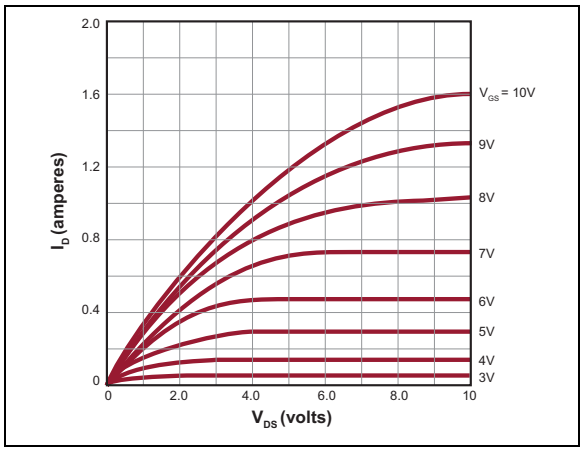


FIGURE 2-10: *Saturation Characteristics.*

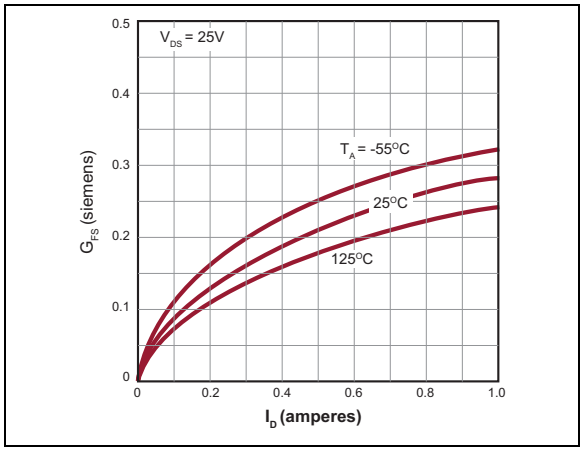


FIGURE 2-8: *Transconductance vs. Drain Current.*

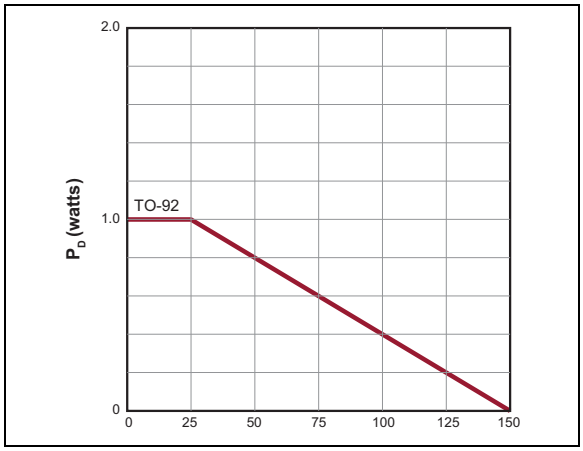


FIGURE 2-11: *Power Dissipation vs. Case Temperature.*

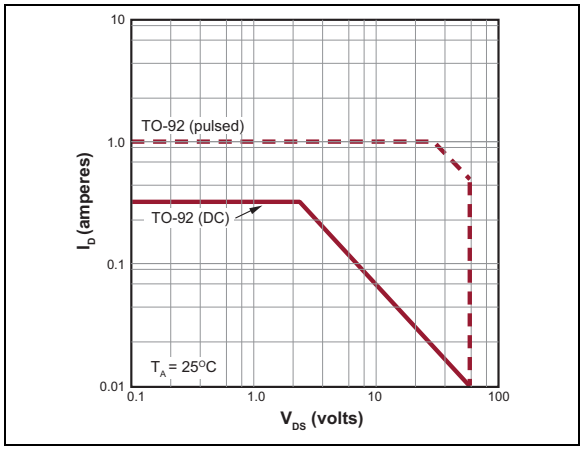


FIGURE 2-9: *Maximum Rated Safe Operating Area.*

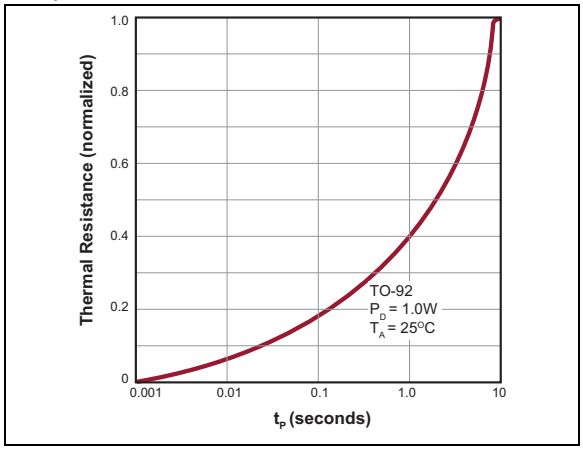


FIGURE 2-12: *Thermal Response Characteristics.*

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3.0 PIN DESCRIPTION

The details on the pins are listed in Table 3-1. Refer to **Package Type** for the location of the pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Controls whether the channel is ON or OFF.
2	Source	Input terminal of the device (connect to the power supply).
3	Drain	Output terminal of the device (delivers current to the load).

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4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for VN2110.

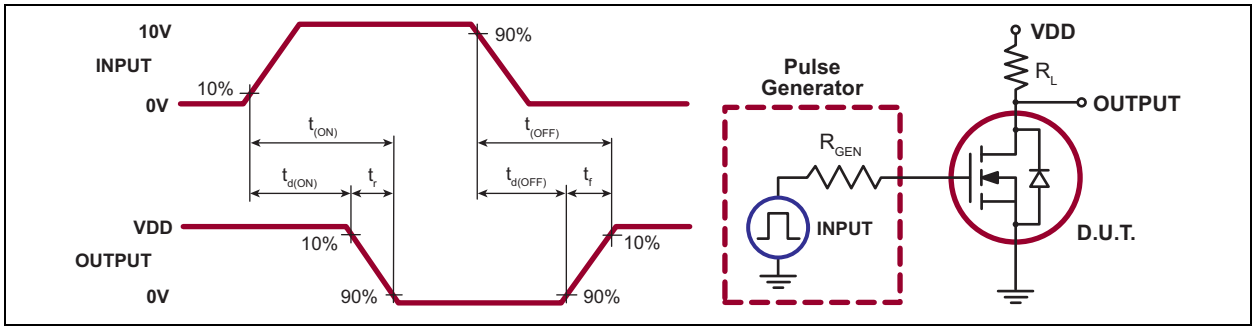


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

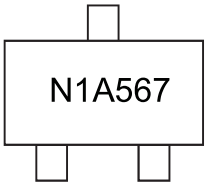
TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)
100	4

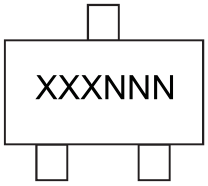
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

3-Lead SOT-23:



Example:



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

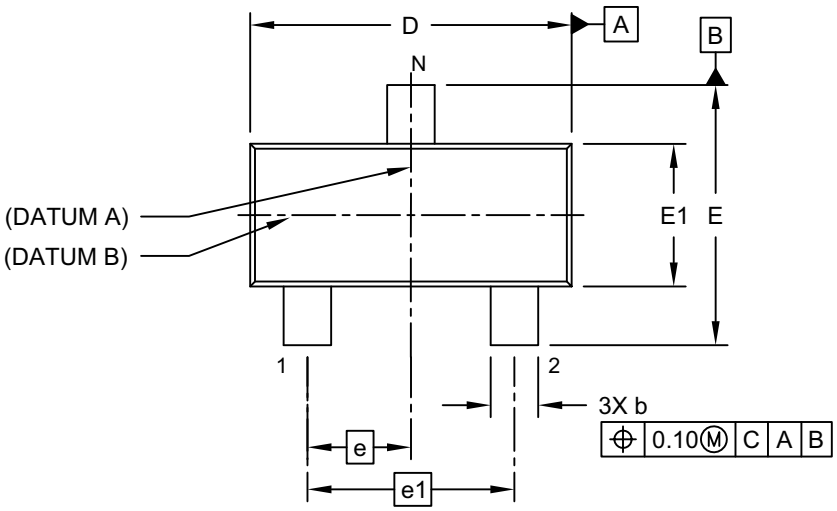
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

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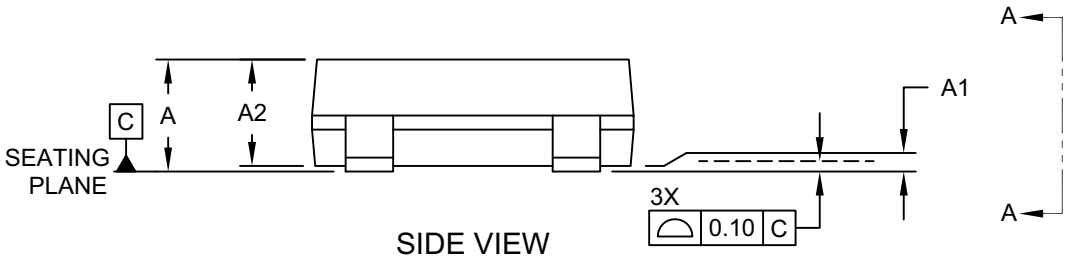
5.2 Package Outline Drawings

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

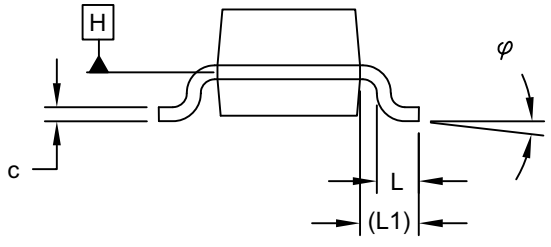
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



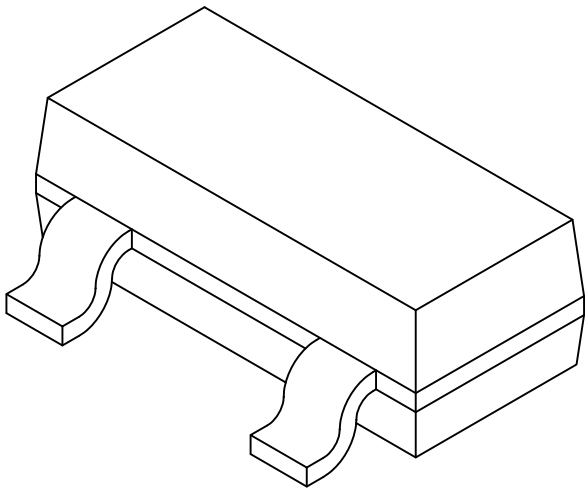
VIEW A-A

Microchip Technology Drawing C04-104 (TT) Rev C Sheet 1 of 2

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3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.89	-	1.12
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	-	0.10
Overall Width	E	2.10	-	2.64
Molded Package Width	E1	1.16	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Footprint	(L1)		0.42 REF	
Foot Angle	φ	0°	-	10°
Lead Thickness	c	0.08	-	0.20
Lead Width	b	0.30	-	0.54

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

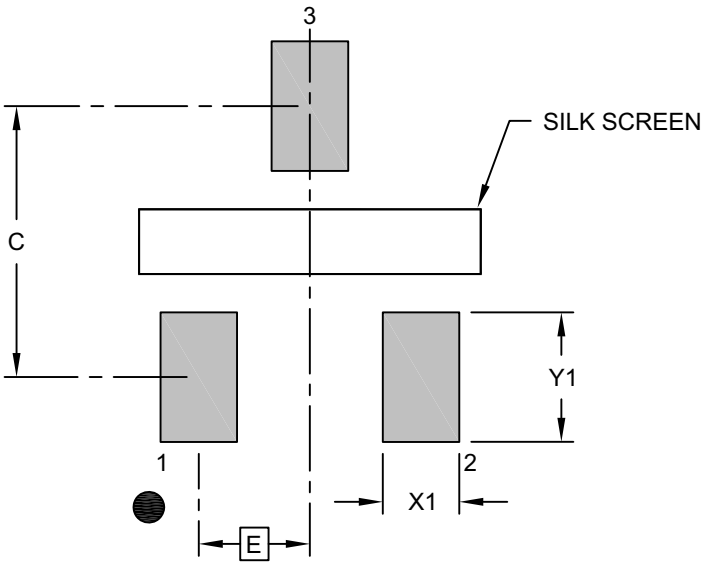
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-104 (TT) Rev C Sheet 2 of 2

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3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.30	
Contact Pad Width (X3)	X1			0.65
Contact Pad Length (X3)	Y1			1.10

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2104 (TT) Rev B

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APPENDIX A: REVISION HISTORY

Revision B (October 2026)

- Updated Pin Function Table to accurately describe the device.
- Updated drawings in **Section 5.0 "Packaging Information"**.

Revision A (September 2021)

- Converted Supertex Doc# DSFP-VN2110 to Microchip DS20005793A.
- Changed the package marking format.
- Made minor text changes throughout the document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	VN2110	=	N-Channel Enhancement-Mode Vertical DMOS FET
Package:	K1	=	3-lead SOT-23
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3000/Reel for a K1 Package

Example:

a) VN2110K1-G: N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-23, 3000/Reel

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