NOMINAL SIZE =   0.75 in x 0.5 in
(19,05 mm x 12,7 mm)

Features

- Up to 6-A Output Current
- 12-V Input Voltage
- Wide-Output Voltage Adjust (1.2 V to 5.5 V)/(0.8 V to 1.8 V)
- 230 W/in³ Power Density
- Efficiencies up to 92 %
- Pre-Bias Startup
- On/Off Inhibit
- Under-Voltage Lockout
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Operating Temp: –40 to +85 °C
- Surface Mount Package
- Safety Agency Approvals: UL/cUL 60950, EN60950 VDE (Pending)

Description

The PTH12000 series of non-isolated power modules are small in size and high on performance. Using double-sided surface mount construction and synchronous rectification technology, these regulators deliver up to 6 A of output current while occupying a PCB area of about half the size of a standard postage stamp. They are an ideal choice for applications where space, performance and cost are important design constraints.

The series operates from an input voltage of 12 V to provide step-down power conversion to a wide range of output voltages. W-suffix devices are adjustable from 1.2 V to 5.5 V, and L-suffix devices are adjustable from 0.8 V to 1.8 V. The output voltage is set within the adjustment range using a single external resistor.

Operating features include an on/off inhibit, output voltage adjust (trim), and the ability to start up into an existing output voltage or prebias. A non-latching over-current trip provides protection against load faults.

Target applications include telecom, industrial, and general purpose circuits, including low-power dual-voltage systems that use a DSP, microprocessor, or ASIC.

Package options include both through-hole and surface mount configurations.

Pin Configuration

Pin	Function
1	GND
2	V_{in}
3	Inhibit *
4	V_o Adjust
5	V_{out}

* *Denotes negative logic:*
Open   = Output On
Ground = Output Off

Standard Application

R_{set} = Required to set the output voltage higher than the lowest value (see spec. table for values).
C_1 = Required 100 µF capacitor
C_2 = Optional 100 µF capacitor
C_3 = Optional 10 µF ceramic capacitor

**6-A, 12-V Input Non-Isolated
Wide-Output Adjust Power Module**
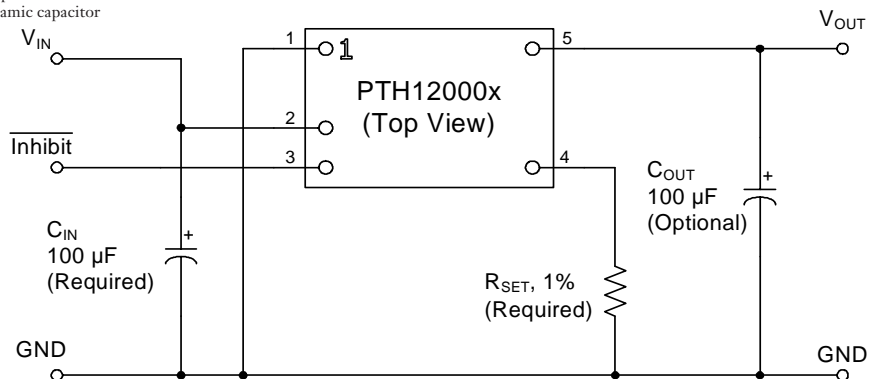
Ordering Information

Output Voltage (PTH12000☐xx)		Package Options (PTH12000x☐☐) [1]		
Code	**Voltage**	**Code**	**Description**	**Pkg Ref.** [2]
W	1.2 V – 5.5 V (Adjust)	AH	Horiz. T/H	(EUS)
L	0.8 V – 1.8 V (Adjust)	AS	SMD, Standard [3]	(EUT)

Notes: *(1) Add "T" to end of part number for tape and reel on SMD packages only.*
(2) Reference the applicable package reference drawing for the dimensions and PC board layout
(3) "Standard" option specifies 63/37, Sn/Pb pin solder material.

Pin Descriptions

Vin: The positive input voltage power node to the module, which is referenced to common GND.

Vout: The regulated positive power output with respect to the GND node.

GND: This is the common ground connection for the 'V$_{in}$' and 'V$_{out}$' power connections. It is also the 0 VDC reference for the 'Inhibit' and 'V$_o$ Adjust' control inputs.

Inhibit: The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

Vo Adjust: A 1-% resistor must be connected between this pin and GND (pin 1) to set the output voltage of the module higher than its lowest value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 1.2 V to 5.5 V for W-suffix devices, and 0.8 V to 1.8 V for L-suffix devices. The resistor value required for a given output voltage may be calculated using a formula. If left open circuit, the output voltage will default to its lowest value. For further information on output voltage adjustment consult the related application note.

The specification tables also give the preferred resistor values for a number of standard output voltages.

Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

| Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Operating Temperature Range	T$_a$	Over V$_{in}$ Range	–40 [i]	—	+85	°C
Solder Reflow Temperature	T$_{reflow}$	Surface temperature of module body or pins			235 [ii]	°C
Storage Temperature	T$_s$	—	–40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ sine, mounted	—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	—	15	—	G's
Weight	—		—	2	—	grams
Flammability	—	Meets UL 94V-O				

Notes: *(i) For operation below 0 °C the external capacitors must have stable characteristics. Use either a low ESR tantalum, Oscon, or ceramic capacitor.*
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

**6-A, 12-V Input Non-Isolated
Wide-Output Adjust Power Module**

Electrical Specifications

Unless otherwise stated, $T_a = 25$ °C, $V_{in} = 12$ V, $V_o = 3.3$ V, $C_1 = 100$ µF, $C_2 = 0$ µF, $C_3 = 0$ µF, and $I_o = I_o$max

Characteristics	Symbols	Conditions		Min	Typ	Max	Units
Output Current	I_o	Over ΔV_{adj} range	$T_a = 60$ °C, 200 LFM	0	—	6 (1)	A
			$T_a = 25$ °C, natural convection	0	—	6 (1)	
Input Voltage Range	V_{in}	Over I_o range		10.8	—	13.2	V
Set-Point Voltage Tolerance	V_o tol			—	—	±2 (2)	%V_o
Temperature Variation	ΔReg_{temp}	–40 °C < T_a < +85 °C		—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range		—	±5	—	mV
Load Regulation	ΔReg_{load}	Over I_o range		—	±5	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_a ≤ +85 °C		—	—	±3 (2)	%V_o
Ouput Voltage Adjust Range	ΔV_{adj}	Over V_{in} range		1.2	—	5.5	V
Efficiency	η	$V_{in} = 12$ V, $I_o = 4$ A	$R_{SET} = 280$ Ω $V_o = 5.0$ V	—	92	—	%
			$R_{SET} = 2.0$ kΩ $V_o = 3.3$ V	—	90	—	
			$R_{SET} = 4.32$ kΩ $V_o = 2.5$ V	—	88	—	
			$R_{SET} = 8.06$ kΩ $V_o = 2.0$ V	—	87	—	
			$R_{SET} = 11.5$ kΩ $V_o = 1.8$ V	—	86	—	
			$R_{SET} = 24.3$ kΩ $V_o = 1.5$ V	—	84	—	
			R_{SET} = open cct $V_o = 1.2$ V	—	82	—	
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth, $I_o = 4$ A $V_o \geq 3.3$ V		—	50 (3)	—	mVpp
		$C_3 = 10$ µF ceramic $V_o \leq 2.5$ V		—	25 (3)	—	
Transient Response		1 A/µs load step, 50 to 100 % $I_o$max, $V_o = 1.8$ V, $C_2 = 100$ µF					
	t_{tr}	Recovery time		—	70	—	µSec
	ΔV_{tr}	V_o over/undershoot		—	100	—	mV
Over-Current Threshold	I_o trip	Reset followed by auto-recovery		—	12	—	A
Under-Voltage Lockout	UVLO	V_{in} increasing		—	—	10.4	V
		V_{in} decreasing		8.8	—	—	
Inhibit Control (pin 3)		Referenced to GND					
Input High Voltage	V_{IH}			$V_{in} –0.5$	—	Open (4)	V
Input Low Voltage	V_{IL}			–0.2	—	0.5	
Input Low Current	I_{IL}	Pin 3 to GND		—	–240	—	µA
Standby Input Current	I_{in} standby	pins 1 & 3 connected		—	1	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges		300	350	400	kHz
External Input Capacitance	C_{in}			100 (5)	—	—	µF
External Output Capacitance	C_{out}	Capacitance value non-ceramic		0	100 (6)	3,300 (7)	µF
		ceramic		0	—	300	
		Equiv. series resistance (non-ceramic)		4 (8)	—	—	mΩ
Reliability	MTBF	Per Bellcore TR-332 50 % stress, $T_a = 40$ °C, ground benign		9.4	—	—	10^6 Hrs

Notes:
(1) See SOA curves or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(3) The pk-pk output ripple voltage is measured with an external 10 µF ceramic capacitor. See the standard application schematic.
(4) The Inhibit control (pin 3) has an internal pull-up to Vin, and if left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended to control this input. See application notes for more information.
(5) The regulator requires a minimum of 100 µF input capacitor with a minimum 750 mArms ripple current rating. For further information, consult the related application note on Capacitor Recommendations.
(6) An external output capacitor is not required for basic operation. Adding 100 µF of distributed capacitance at the load will improve the transient response.
(7) This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult the application notes for further guidance.
(8) This is the typical ESR for all the electrolytic (non-ceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

TEXAS INSTRUMENTS
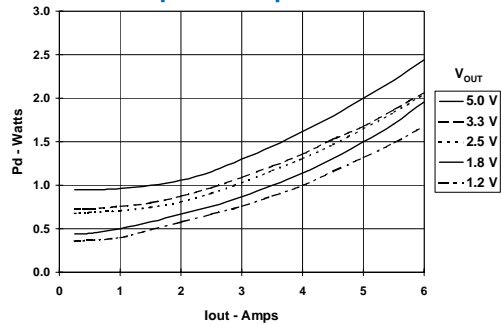
PTH12000W Characteristic Data; V_{in} =12 V *(See Note A)*

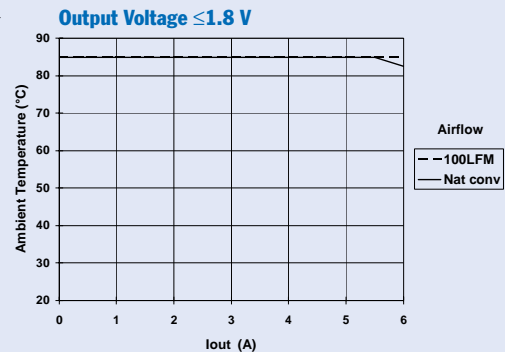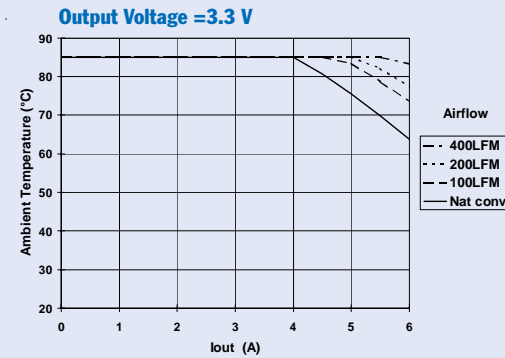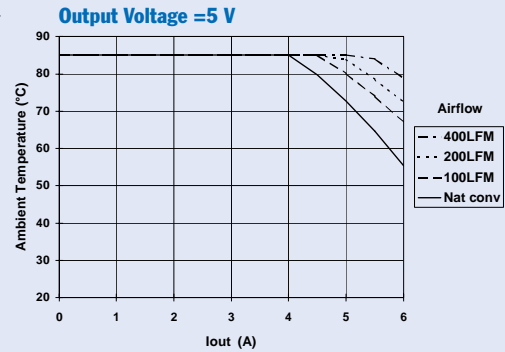**Efficiency vs Output Current**
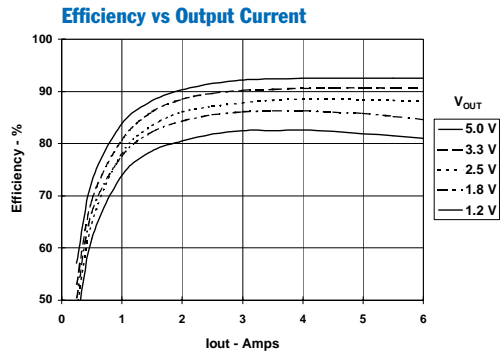
Output Ripple vs Load Current (See Note 3 to Table)
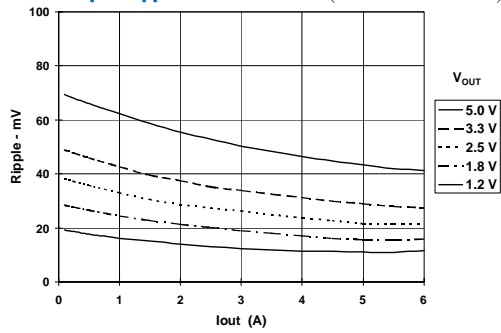
Power Dissipation vs Output Current

PTH12000W Safe Operating Area; V_{in} =12 V *(See Note B)*

Output Voltage =5 V

Output Voltage =3.3 V

Output Voltage ≤1.8 V

Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*
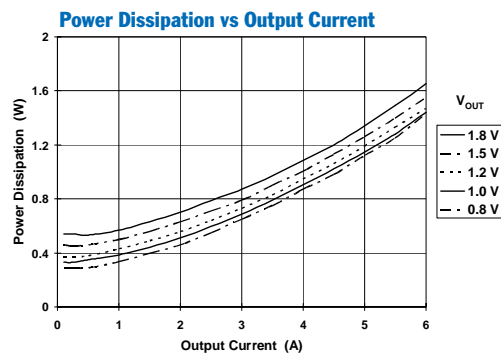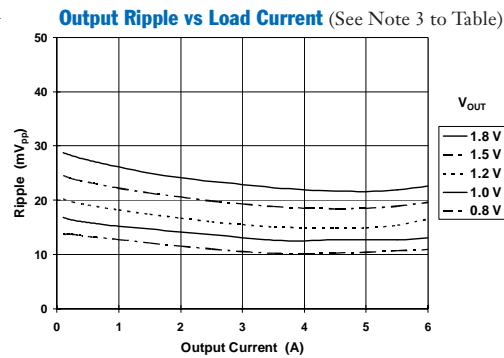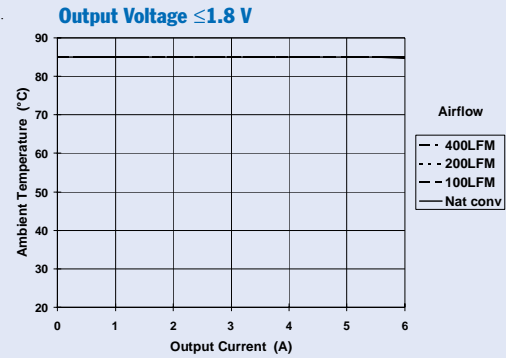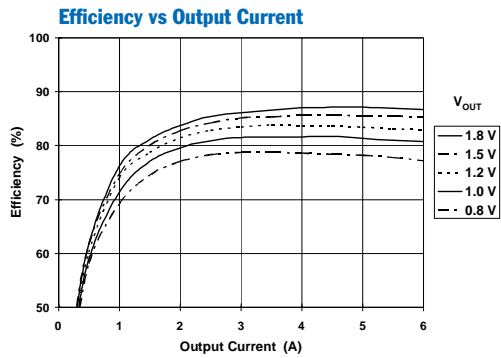
TEXAS INSTRUMENTS

For technical support and further information visit http://power.ti.com

6-A, 12-V Input Non-Isolated
Wide-Output Adjust Power Module

Electrical Specifications
Unless otherwise stated, $T_a = 25\ ^\circ C$, $V_{in} = 12\ V$, $V_o = 1.8\ V$, $C_1 = 100\ \mu F$, $C_2 = 0\ \mu F$, $C_3 = 0\ \mu F$, and $I_o = I_o max$

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
				PTH12000L		
Output Current	I_o	Over ΔV_{adj} range, $\qquad T_a = 85\ ^\circ C$, natural convection	0	—	6	A
Input Voltage Range	V_{in}	Over I_o range	10.8	—	13.2	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2 (1)	$\%V_o$
Temperature Variation	ΔReg_{temp}	$-40\ ^\circ C < T_a < +85\ ^\circ C$	—	±0.5	—	$\%V_o$
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±5	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±5	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, $-40\ ^\circ C \leq T_a \leq +85\ ^\circ C$	—	—	±3 (1)	$\%V_o$
Ouput Voltage Adjust Range	ΔV_{adj}	Over V_{in} range	0.8	—	1.8	V
Efficiency	η	$V_{in} = 12\ V$, $I_o = 4\ A$ $\quad R_{SET} = 130\ \Omega \quad V_o = 1.8\ V$ $R_{SET} = 3.57\ k\Omega\ \ V_o = 1.5\ V$ $R_{SET} = 12.1\ k\Omega\ \ V_o = 1.2\ V$ $R_{SET} = 32.4\ k\Omega\ \ V_o = 1.0\ V$ $R_{SET} = Open\ cct\ V_o = 0.8\ V$	— — — — —	87 86 85 82 79	— — — — —	%
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth, $I_o = 4\ A$ $\quad V_o > 1.2\ V$ $C_3 = 10\ \mu F$ ceramic $\qquad V_o \leq 1.2\ V$	— —	25 (2) 20 (2)	— —	mVpp
Transient Response	t_{tr} ΔV_{tr}	1 A/μs load step, 50 to 100 % $I_o$max, $V_o = 1.8\ V$, $C_2 = 100\ \mu F$ Recovery time V_o over/undershoot	— —	70 100	— —	μSec mV
Over-Current Threshold	I_o trip	Reset followed by auto-recovery	—	12	—	A
Under-Voltage Lockout	UVLO	V_{in} increasing V_{in} decreasing	— 8.8	— —	10.4 —	V
Inhibit Control (pin 3) Input High Voltage Input Low Voltage	V_{IH} V_{IL}	Referenced to GND	$V_{in} - 0.5$ -0.2	— —	Open (3) 0.5	V
Input Low Current	I_{IL}	Pin 3 to GND	—	−240	—	μA
Standby Input Current	I_{in} standby	pins 1 & 3 connected	—	1	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges	200	250	300	kHz
External Input Capacitance	C_{in}		100 (4)	—	—	μF
External Output Capacitance	C_{out}	Capacitance value $\qquad$ non-ceramic ceramic	0 0	100 (5) —	3,300 (6) 300	μF
		Equiv. series resistance (non-ceramic)	4 (7)	—	—	mΩ
Reliability	MTBF	Per Bellcore TR-332 50 % stress, $T_a = 40\ ^\circ C$, ground benign	9.4	—	—	10^6 Hrs

Notes: (1) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.

(2) The pk-pk output ripple voltage is measured with an external 10 μF ceramic capacitor. See the standard application schematic.

(3) The Inhibit control (pin 3) has an internal pull-up to Vin, and if left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended to control this input. See application notes for more information.

(4) The regulator requires a minimum of 100 μF input capacitor with a minimum 750 mArms ripple current rating. For further information, consult the related application note on Capacitor Recommendations.

(5) An external output capacitor is not required for basic operation. Adding 100 μF of distributed capacitance at the load will improve the transient response.

(6) This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult the application notes for further guidance.

(7) This is the typical ESR for all the electrolytic (non-ceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

TEXAS INSTRUMENTS

PTH12000L Characteristic Data, V_{in} =12 V *(See Note A)*

Efficiency vs Output Current

Efficiency (%) vs Output Current (A)

V_{OUT}
- 1.8 V
- 1.5 V
- 1.2 V
- 1.0 V
- 0.8 V

Output Ripple vs Load Current (See Note 3 to Table)

Ripple (mV_{pp}) vs Output Current (A)

V_{OUT}
- 1.8 V
- 1.5 V
- 1.2 V
- 1.0 V
- 0.8 V

Power Dissipation vs Output Current

Power Dissipation (W) vs Output Current (A)

V_{OUT}
- 1.8 V
- 1.5 V
- 1.2 V
- 1.0 V
- 0.8 V

PTH12000L Safe Operating Area; V_{in} =12 V *(See Note B)*

Output Voltage ≤1.8 V

Ambient Temperature (°C) vs Output Current (A)

Airflow
- 400LFM
- 200LFM
- 100LFM
- Nat conv

Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*

Capacitor Recommendations for the PTH12000 Wide-Output Adjust Power Modules

Input Capacitor

The recommended input capacitance is determined by the 100 µF minimum capacitance and 750 mArms minimum ripple current rating. A 10-µF X5R/X7R ceramic capacitor may also be added to reduce the reflected input ripple current [3]. The ceramic capacitor should be located between the input electrolytic and the module.

Ripple current, less than 150 mΩ equivalent series resistance (ESR) and temperature are major considerations when selecting input capacitors. Unlike polymer-tantalum capacitors, regular tantalum capacitors have a recommended minimum voltage rating of 2 × (max. DC voltage + AC ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with sufficient voltage rating to meet this requirement. At temperatures below 0 °C, the ESR of aluminum electrolytic capacitors increases. For these applications Os-Con, polymer-tantalum, and polymer-aluminum types should be considered.

Output Capacitors (Optional)

For applications with load transients (sudden changes in load current), regulator response will benefit from external output capacitance. The value of 100 µF is used to define the transient response specification (see data sheet). For most applications, a high quality computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable for ambient temperatures above 0 °C. Below 0 °C, tantalum, ceramic or Os-Con type capacitors are recommended. When using one or more non-ceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 1-1.

In addition to electrolytic capacitance, adding a 10-µF X5R/X7R ceramic capacitor to the output will reduce the output ripple voltage and improve the regulator's transient response. The measurement of both the output ripple and transient response is also best achieved across a 10-µF ceramic capacitor.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input [3] and improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum type capacitors are most suited for use on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0 °C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution many general purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit will be encountered well before the maximum capacitance value is reached.

Capacitor Table

Table 1-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Designing for Very Fast Load Transients

The transient response of the DC/DC converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any DC/DC converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the data sheet, the selection of output capacitors becomes more important.

TEXAS INSTRUMENTS

Table 1-1: Input/Output Capacitors

Capacitor Vendor/ Type Series (Style)	Capacitor Characteristics					Quantity		Vendor Number
	Working Voltage	Value (µF)	Max. ESR @ 100 kHz	Max. Ripple at 85 °C Current (Irms)	Physical Size (mm)	Input Bus	Output Bus	
Panasonic, Aluminum	25 V	330 µF	0.090 Ω	755 mA	10×12.5	1	1	EEUFC1E331
FC (Radial)	35 V	180 µF	0.090 Ω	755 mA	10×12.5	1	1	EEUFC1V181
FK (SMD)	25 V	470 µF	0.080 Ω	850 mA	10×10.2	1	1	EEVFK1E471P
United Chemi-con								
PXA, Poly-Aluminum (SMD)	16 V	150 µF	0.026 Ω	3430 mA	10×7.7	1	≤4	PXA16VC151MJ80TP
FP, Os-con (Radial)	20 V	120 µF	0.024 Ω	3100 mA	8×10.5	1	≤4	20FP120MG
FS, Os-con (Radial)	20 V	100 µF	0.030 Ω	2740 mA	8×10.5	1	≤4	20FS100M
LXZ, Aluminum (Radial)	35 V	220 µF	0.090 Ω	760 mA	10×12.5	1	1	LXZ35VB221M10X12LL
Nichicon Aluminum								
HD, (Radial)	25 V	220 µF	0.072 Ω	760 mA	8×11.5	1	1	UHD1E221MPR
PM, (Radial)	35 V	220 µF	0.090 Ω	770 mA	10×15	1	1	UPM1V221MHH6
Panasonic, Poly-Aluminum:								
WA (SMD)	16 V	100 µF	0.039 Ω	2500 mA	8×6.9	1	≤5	EEFWA1C101P
S/SE (SMD)	6.3 V	180 µF	0.005 Ω	4000 mA	7.3×4.3×4.2	N/R [2]	≤1 [1]	EEFSE0J181R **(V$_o$ ≤5.1V)**
Sanyo								
SVP, Os-con (SMD)	20 V	100 µF	0.024 Ω	>3300 mA	8×12	1	≤4	20SVP100M
SP, Os-con (Radial)	20 V	120 µF	0.024 Ω	>3100 mA	8×10.5	1	≤4	20SP120M
TPE, Pos-Ccap (SMD)	10 V	220 µF	0.025 Ω	>2400 mA	7.3×5.7	1	≤4	10TPE220ML
AVX, Tantalum TPS (SMD)	10 V	100 µF	0.100 Ω	>1090 mA	7.3L	N/R [2]	≤5	TPSD107M010R0100
	10 V	220 µF	0.100 Ω	>1414 mA	×4.3W	N/R [2]	≤5	TPSV227M010R0100
	25 V	68 µF	0.095 Ω	>1451 mA	×4.1H	2	≤5	TPSV686M025R0095
Kemet								
T520, Poy-Tant (SMD)	10 V	100 µF	0.080 Ω	1200 mA	7.3L×5.7W	N/R [2]	≤5	T520D107M010AS
T495, Tantalum (SMD)	10 V	100 µF	0.100 Ω	>1100 mA	×4.0H	N/R [2]	≤5	T495X107M010AS
Vishay-Sprague								
594D, Tantalum (SMD)	10 V	150 µF	0.090 Ω	1100 mA	7.3L×6.0W	N/R [2]	≤5	594D157X0010C2T
	25 V	68 µF	0.095 Ω	1600 mA	×4.1H	2	≤5	594D686X0025R2T
94SP, Organic (Radial)	16 V	100 µF	0.070 Ω	2890 mA	10×10.5	1	≤5	94SP107X0016FBP
Kemet, Ceramic X5R (SMD)	16 V	10 µF	0.002 Ω	—	1210 case	1 [3]	≤5	C1210C106M4PAC
	6.3 V	47 µF	0.002 Ω		3225 mm	N/R [2]	≤5 [1]	C1210C476K9PAC **(V$_o$ ≤5.1V)**
Murata, Ceramic X5R (SMD)	6.3 V	100 µF	0.002 Ω	—	1210 case	N/R [2]	≤3 [1]	GRM32ER60J107M **(V$_o$ ≤5.1V)**
	6.3 V	47 µF			3225 mm	N/R [2]	≤5 [1]	GRM32ER60J476M **(V$_o$ ≤5.1V)**
	16 V	22 µF				1 [3]	≤5	GRM32ER61C226K
	16 V	10 µF				1 [3]	≤5	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 V	100 µF	0.002 Ω	—	1210 case	N/R [2]	≤3 [1]	C3225X5R0J107MT **(V$_o$ ≤5.1V)**
	6.3 V	47 µF			3225 mm	N/R [2]	≤5 [1]	C3225X5R0J476MT **(V$_o$ ≤5.1V)**
	16 V	22 µF				1 [3]	≤5	C3225X5R1C226MT
	16 V	10 µF				1 [3]	≤5	C3225X5R1C106MT

[1] The voltage rating of this capacitor only allows it to be used for output voltages that are equal to or less than 5.1 V
[2] N/R –Not recommended. The capacitor voltage rating does not meet the minimum derated operating limits.
[3] A ceramic capacitor may be used to complement electrolytic types at the input to further reduce high-frequency ripple current.

Adjusting the Output Voltage of the PTH12000x Wide-Output Adjust Power Modules

The *V$_o$ Adjust* control (pin 4) sets the output voltage of the PTH12000 product. The adjustment range is from 1.2 V to 5.5 V for the W-suffix modules, and 0.8 V to 1.8 V for L-suffix modules. The adjustment method requires the addition of a single external resistor, R$_{set}$, that must be connected directly between the *V$_o$ Adjust* and *GND* pins [1]. Table 2-1 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides. Figure 2-1 shows the placement of the required resistor.

Table 2-1; Preferred Values of R$_{set}$ for Standard Output Voltages

| V$_{out}$ (Req'd)	PTH12000W		PTH12000L	
	R$_{set}$	V$_{out}$ (Actual)	R$_{set}$	V$_{out}$ (Actual)
5 V	280 Ω	5.009 V	N/A	N/A
3.3 V	2.0 kΩ	3.294 V	N/A	N/A
2.5 V	4.32 kΩ	2.503 V	N/A	N/A
2 V	8.06 kΩ	2.010 V	N/A	N/A
1.8 V	11.5 kΩ	1.801 V	130 Ω	1.800 V
1.5 V	24.3 kΩ	1.506 V	3.57 kΩ	1.499 V
1.2 V	Open	1.200 V	12.1 kΩ	1.201 V
1.1 V	N/A	N/A	18.7 kΩ	1.101 V
1.0 V	N/A	N/A	32.4 kΩ	0.999 V
0.9 V	N/A	N/A	71.5 kΩ	0.901 V
0.8 V	N/A	N/A	Open	0.800 V

For other output voltages the value of the required resistor can either be calculated, or simply selected from the range of values given in Table 2-3. The following formula may be used for calculating the adjust resistor value. Select the appropriate value for the parameters, R$_s$ and V$_{min}$, from Table 2.2.

$$R_{set} = 10\,k\Omega \cdot \frac{0.8\,V}{V_{out} - V_{min}} - R_s \quad k\Omega$$

Table 2.2; Adjust Formula Parameters

Pt. No.	PTH12000W	PTH12000L
V$_{min}$	1.2 V	0.8 V
V$_{max}$	5.5 V	1.8 V
R$_s$	1.82 kΩ	7.87 kΩ

Figure 2-1; V$_o$ Adjust Resistor Placement
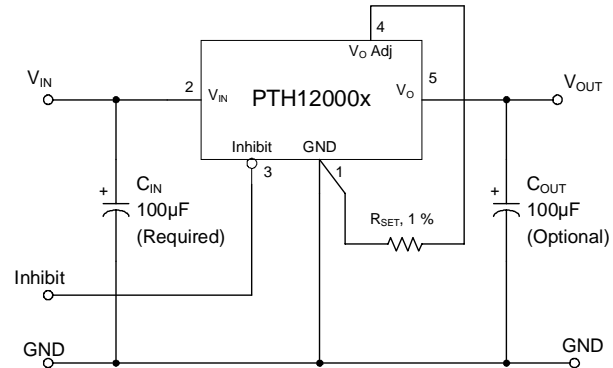
Notes:
1. A 0.05-W rated resistor may be used. The tolerance should be 1 %, with a temperature stability of 100 ppm/°C or better. Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 1 using dedicated PCB traces.

2. Never connect capacitors from *V$_o$ Adjust* to either *GND* or *V$_{out}$*. Any capacitance added to the *V$_o$ Adjust* pin will affect the stability of the regulator.

TEXAS INSTRUMENTS

PTH12000 Series

Table 2-3; Output Voltage Set-Point Resistor Values

PTH12000W				PTH12000L	
V_{OUT}	R_{SET}	V_{OUT}	R_{SET}	V_{OUT}	R_{SET}
1.200	Open	2.70	3.51 kΩ	0.800	Open
1.225	318.0 kΩ	2.75	3.34 kΩ	0.825	312.0 kΩ
1.250	158.0 kΩ	2.80	3.18 kΩ	0.850	152.0 kΩ
1.275	105.0 kΩ	2.85	3.03 kΩ	0.875	98.8 kΩ
1.300	78.2 kΩ	2.90	2.89 kΩ	0.900	72.1 kΩ
1.325	62.2 kΩ	2.95	2.75 kΩ	0.925	56.1 kΩ
1.350	51.5 kΩ	3.00	2.62 kΩ	0.950	45.5 kΩ
1.375	43.9 kΩ	3.05	2.50 kΩ	0.975	37.8 kΩ
1.400	38.2 kΩ	3.10	2.39 kΩ	1.000	32.1 kΩ
1.425	33.7 kΩ	3.15	2.28 kΩ	1.025	27.7 kΩ
1.450	30.2 kΩ	3.20	2.18 kΩ	1.050	24.1 kΩ
1.475	27.3 kΩ	3.25	2.08 kΩ	1.075	21.2 kΩ
1.50	24.8 kΩ	3.30	1.99 kΩ	1.100	18.8 kΩ
1.55	21.0 kΩ	3.35	1.90 kΩ	1.125	16.7 kΩ
1.60	18.2 kΩ	3.40	1.82 kΩ	1.150	15.0 kΩ
1.65	16.0 kΩ	3.50	1.66 kΩ	1.175	13.5 kΩ
1.70	14.2 kΩ	3.60	1.51 kΩ	1.200	12.1 kΩ
1.75	12.7 kΩ	3.70	1.38 kΩ	1.225	11.0 kΩ
1.80	11.5 kΩ	3.80	1.26 kΩ	1.250	9.91 kΩ
1.85	10.5 kΩ	3.90	1.14 kΩ	1.275	8.97 kΩ
1.90	9.61 kΩ	4.00	1.04 kΩ	1.300	8.13 kΩ
1.95	8.85 kΩ	4.10	939 Ω	1.325	7.37 kΩ
2.00	8.18 kΩ	4.20	847 Ω	1.350	6.68 kΩ
2.05	7.59 kΩ	4.30	761 Ω	1.375	6.04 kΩ
2.10	7.07 kΩ	4.40	680 Ω	1.400	5.46 kΩ
2.15	6.60 kΩ	4.50	604 Ω	1.425	4.93 kΩ
2.20	6.18 kΩ	4.60	533 Ω	1.450	4.44 kΩ
2.25	5.80 kΩ	4.70	466 Ω	1.475	3.98 kΩ
2.30	5.45 kΩ	4.80	402 Ω	1.50	3.56 kΩ
2.35	5.14 kΩ	4.90	342 Ω	1.55	2.8 kΩ
2.40	4.85 kΩ	5.00	285 Ω	1.60	2.13 kΩ
2.45	4.58 kΩ	5.10	231 Ω	1.65	1.54 kΩ
2.50	4.33 kΩ	5.20	180 Ω	1.70	1.02 kΩ
2.55	4.11 kΩ	5.30	131 Ω	1.75	551 Ω
2.60	3.89 kΩ	5.40	85 Ω	1.80	130 Ω
2.65	3.70 kΩ	5.50	41 Ω		

TEXAS INSTRUMENTS

Power-Up Characteristics

When configured per the standard application, the PTH12000x power modules produce a regulated output voltage whenever of a valid input voltage is applied from V_{in} (pin 2), with respect to *GND* (pin 1). During the power-up period, internal soft-start circuitry slows the rate that the output voltage rises. This reduces the in-rush current drawn from the input source. The soft-start circuitry also introduces a short time delay (typically 12 ms) into the power-up characteristic. The delay is from the point that a valid input source is recognized, to the initial rise of the output voltage. Figure 3-1 shows the power-up characteristic of the PTH12000W with the output voltage set to 5-V. The waveforms were measured with a 2-A resistive load. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors.

Figure 3-1

HORIZ SCALE: 5 ms/Div
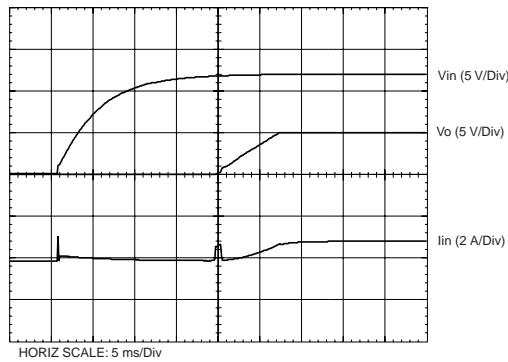
Over-Current Protection

For protectection against load faults, this series incorporates output over-current protection. Applying a load that exceeds the module's over-current threshold will cause the regulated output to shut down. Following shut down the module will periodically attempt to recover by initiating a soft-start power-up. This is often described as a "hiccup" mode of operation, whereby the module continues in the cycle of successive shut down and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Output On/Off Inhibit

The inhibit control (pin 3) is used wherever there is a requirement to turn off the regulator output while input power is applied.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_{in} with respect to *GND*.

Figure 3-2 shows the typical application of the inhibit function. Note the discrete transistor (Q_1). The *Inhibit* pin has its own internal pull-up to V_{in} potential. An open-collector or open-drain device is recommended to control this input.

Turning Q_1 on applies a low voltage to the inhibit control and disables the output of the module. If Q_1 is then turned off, the module will execute a soft-start power-up. A regulated output voltage is produced within 25 msec. Figure 3-3 shows the typical rise in both the output voltage and input current, following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, V_{inh}. The waveforms were measured with a 5-V output and 2-A resistive load.

Figure 3-2

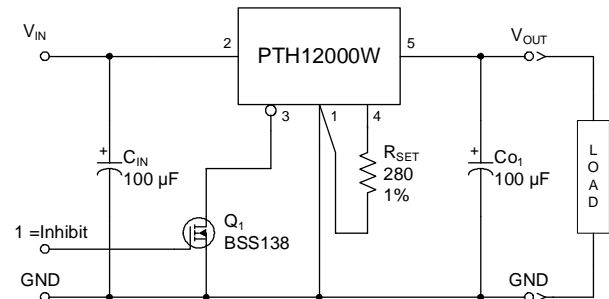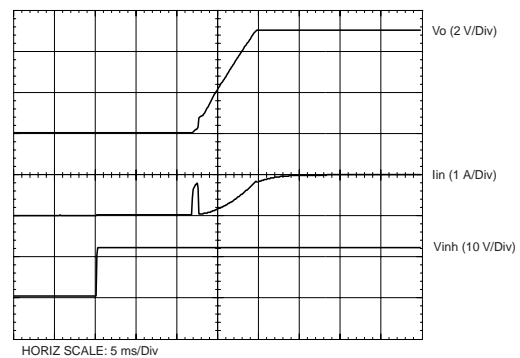

Figure 3-3

HORIZ SCALE: 5 ms/Div

TEXAS INSTRUMENTS

Pre-Bias Startup Capability

The capability to start up into an output pre-bias condition is now a feature of the PTH12000 series of modules. (Note: This is a feature enhancement for the the W-suffix version; see note 1).

A pre-bias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The PTH12000x series of modules incorporate synchronous rectifiers, but will not sink current during startup, or whenever the *Inhibit* pin is held low. Startup includes an initial delay (approx. 8 - 15 ms), followed by the rise of the output voltage under the control of the module's internal soft-start mechanism; see Figure 3-1.

Conditions for Pre-Bias Holdoff

In order for the module to allow an output pre-bias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a pre-bias voltage when the *Inhibit* pin is held low, and whenver the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the *Inhibit* pin (with input voltage applied), or when input power is applied. To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its *Inhibit*), the input voltage must always be greater than the applied pre-bias source. This condition must exist throughout the power-up sequence [3].

The soft-start period is complete when the output begins rising above the pre-bias voltage. Once it is complete the module functions as normal, and will sink current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a pre-bias condition is not present, the soft-start period will be complete when the output voltage has risen to either the set-point voltage.

Demonstration Circuit

The circuit shown in Figure 3-4 is a demonstrates the pre-bias startup feature. Figure 3-5 shows the startup waveforms. The initial rise in Vo_2 is the pre-bias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12000L module (Io_2) is negligible until its output voltage rises above the applied pre-bias.

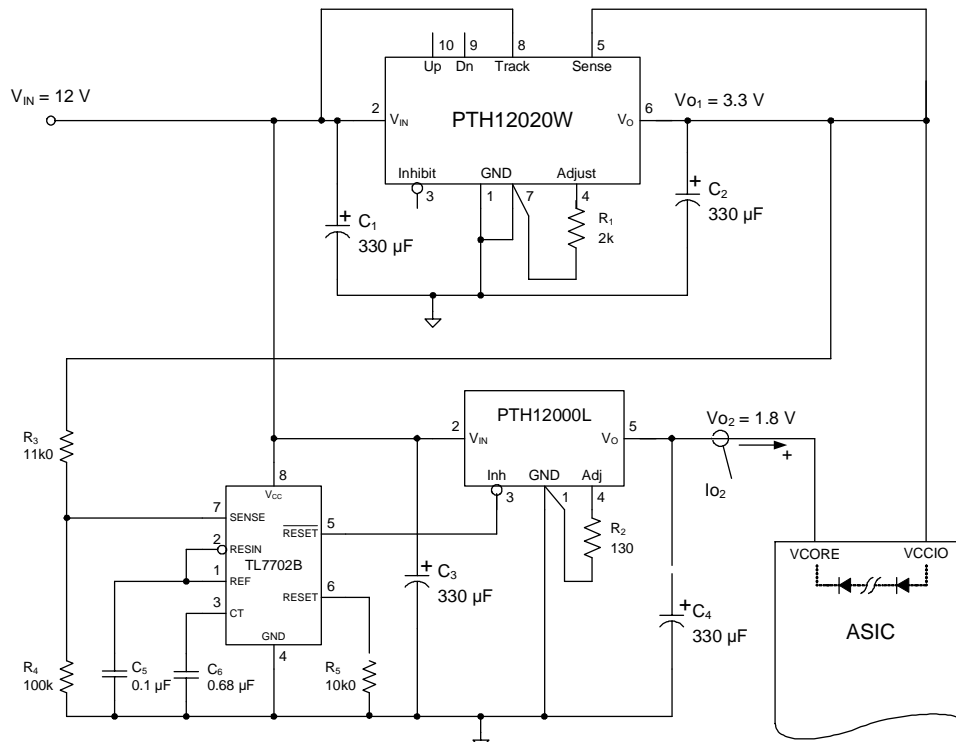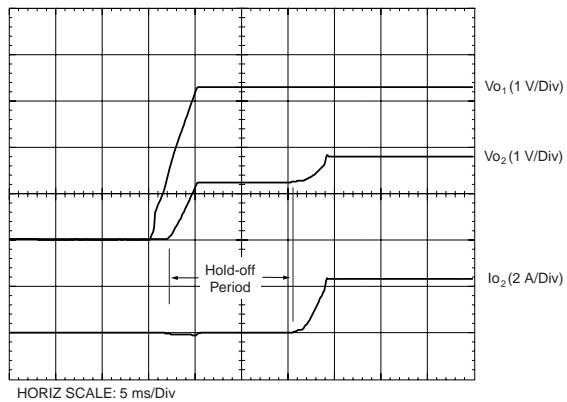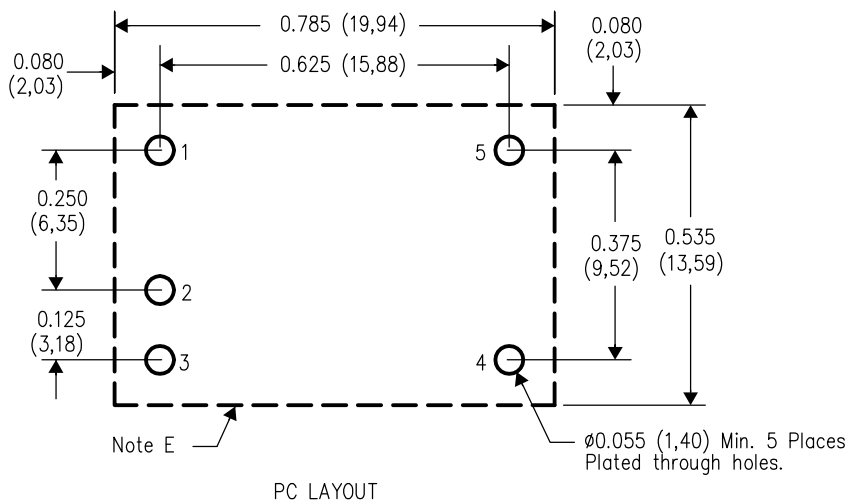*Figure 3–4; Application Circuit Demonstrating Pre-Bias Startup*

Figure 3–5; Pre-Bias Startup Waveforms

Vo_1 (1 V/Div)

Vo_2 (1 V/Div)

Hold-off Period

Io_2 (2 A/Div)

HORIZ SCALE: 5 ms/Div

Notes

1. Output pre-bias holdoff has now been incorporated into the W-suffix modules (PTH12000W), with a production lot date code of "0423" or later.

2. To further ensure that the regulator's output does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage must always be greater than the applied pre-bias source. This condition must exist throughout the power-up sequence of the power system.

TEXAS INSTRUMENTS

Suffix H

0.140
(3,55)

0.745 (18,92)

0.060
(1,52)

0.625 (15,88)

0.060
(1,52)

⌀0.040 (1,02)
5 Places
Note F, G.

1

5

0.250
(6,35)

Lowest Component
0.010 MIN.
(0,25)
Bottom side
Clearance

0.375
(9,52)

0.495
(12,57)

2

0.125
(3,18)

3

4

Host Board

TOP VIEW

0.335 (8,50)
MAX.

SIDE VIEW

0.785 (19,94)

0.080
(2,03)

0.080
(2,03)

0.625 (15,88)

1

5

0.250
(6,35)

0.375
(9,52)

0.535
(13,59)

2

0.125
(3,18)

3

4

Note E

⌀0.055 (1,40) Min. 5 Places
Plated through holes.

PC LAYOUT
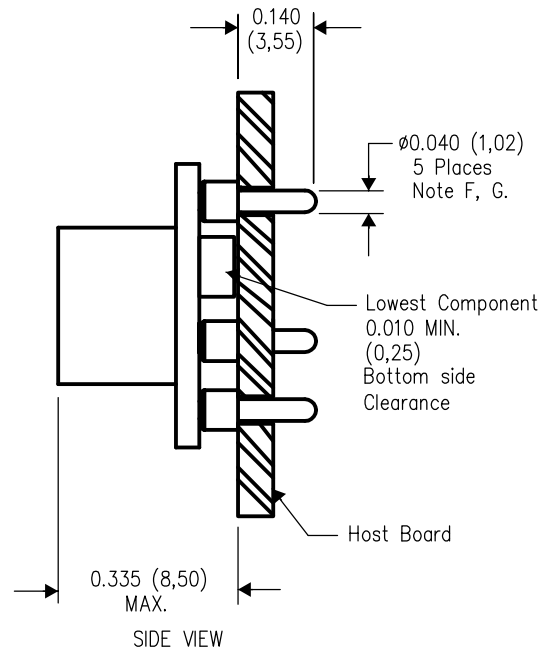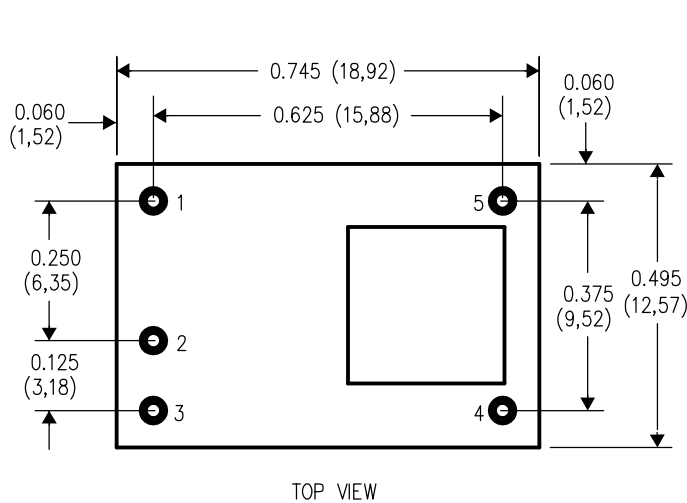
4204990/B 06/03

NOTES: A. All linear dimensions are in inches (mm).
    B. This drawing is subject to change without notice.
    C. 2 place decimals are ±0.030 (±0,76mm).
    D. 3 place decimals are ±0.010 (±0,25mm).
    E. Recommended keep out area for user components.

F. Pins are 0.040" (1,02) diameter with
  0.070" (1,78) diameter standoff shoulder.
G. All pins: Material − Copper Alloy
       Finish − Tin (100%) over Nickel plate

EUT (R−PDSS−B5)   DOUBLE SIDED MODULE

Suffix S

TOP VIEW

SIDE VIEW

Solder Ball
ø0.040 (1,02)
5 Places
Note I

0.358 (9,09)
MAX.
See Note J

0.745 (18,92)
0.625 (15,88)
0.060 (1,52)
0.060 (1,52)
0.250 (6,35)
0.125 (3,18)
0.495
0.375 (12,57)
(9,52)

PC LAYOUT

0.785 (19,94)
0.625 (15,88)
0.080 (2,03)
0.080 (2,03)
0.250 (6,35)
0.125 (3,18)
0.375 (9,52)
0.535 (13,59)

Note E

ø0.085 (2,16) 5 Places
See Note F, G & H

Lowest
Component
0.010 MIN.
(0,25)
Bottom side
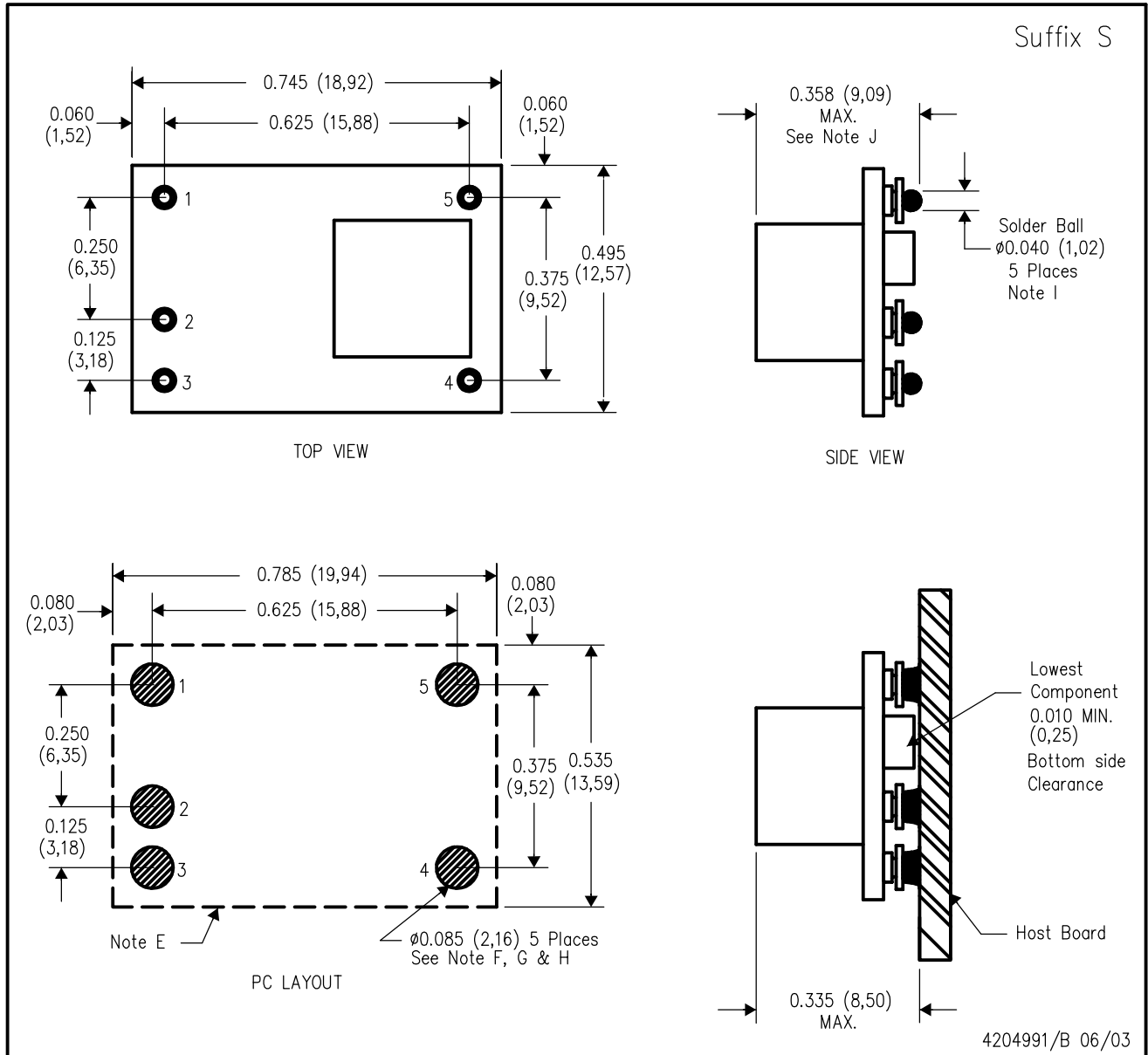Clearance

Host Board

0.335 (8,50)
MAX.

4204991/B 06/03

NOTES: A. All linear dimensions are in inches (mm).
        B. This drawing is subject to change without notice.
        C. 2 place decimals are ±0.030 (±0,76mm).
        D. 3 place decimals are ±0.010 (±0,25mm).
        E. Recommended keep out area for user components.
        F. Power pin connection should utilize two or more vias
            to the interior power plane of 0.025 (0,63) I.D. per input,
            ground and output pin (or the electrical equivalent).

        G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16).
            Paste screen thickness: 0.006 (0,15).
        H. Pad type: Solder mask defined.
        I. All pins: Material − Copper Alloy
            Finish − Tin (100%) over Nickel plate
            Solder Ball − See product data sheet.
        J. Dimension prior to reflow solder.

TEXAS INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
                               Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated