12-A, 12-V Input Non-Isolated Wide-Output Adjust Power Module

SLTS205D - JUNE 2003 - REVISED JUNE 2004

NOMINAL SIZE = 1.37 in x 0.62 in (34,8 mm x 15,75 mm)

Features

- Up to 12-A Output Current
- 12-V Input Voltage
- Wide-Output Voltage Adjust (1.2 V to 5.5 V)/(0.8 V to 1.8 V)
- Efficiencies up to 94 %
- 200 W/in³ Power Density
- On/Off Inhibit
- Output Voltage Sense
- Pre-Bias Startup
- Under-Voltage Lockout
- Auto-Track™ Sequencing
- Margin Up/Down Controls
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Operating Temp: –40 to +85 °C
- Safety Agency Approvals: UL /cUL 60950, EN60950 VDE (Pending)
- Point of Load Alliance (POLA) Compatible

Description

The PTH12010 series of non-isolated power modules that are small in size but big on performance and flexibility. The high output current, compact footprint, and industry-leading features offers system designers a versatile module for powering complex multi-processor digital systems.

The series employs double-sided surface mount construction and provides high-performance step-down power conversion for up to 12 A of output current. The output voltage of the W-suffix parts can be set to any value over the range, 1.2 V to 5.5 V. The L-suffix devices have an adjustment range of 0.8 V to 1.8 V. The output voltage is set using a single external resistor.

This series includes Auto-Track™ sequencing. Auto-Track simplifies the task of supply voltage sequencing in a power system by enabling modules to track each other, or any external voltage, during power up and power down.

Other operating features include an on/off inhibit, output voltage adjust (trim), margin up/down controls, and the ability to start up into an existing output voltage or prebias. For improved load regulation, an output voltage sense is also provided. A non-latching over-current trip serves as load fault protection.

Target applications include complex multi-voltage, multi-processor systems that incorporate the industry's high-speed DSPs, micro-processors and bus drivers.

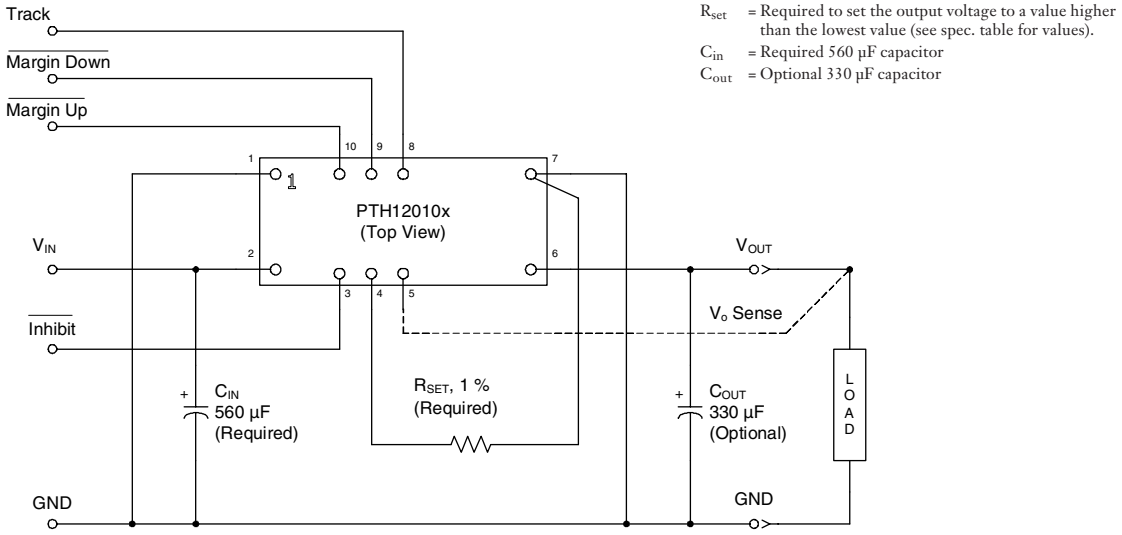
Pin Configuration

Pin	Function
1	GND
2	V_{in}
3	Inhibit *
4	V_o Adjust
5	V_o Sense
6	V_{out}
7	GND
8	Track
9	Margin Down *
10	Margin Up *

* *Denotes negative logic:*
Open = Normal operation
Ground = Function active

Auto-Track™ Sequencing

Standard Application



R_{set} = Required to set the output voltage to a value higher than the lowest value (see spec. table for values).
C_{in} = Required 560 µF capacitor
C_{out} = Optional 330 µF capacitor

Ordering Information

Output Voltage (PTH12010❒xx)

Code	Voltage
W	1.2 V – 5.5 V (Adjust)
L	0.8 V – 1.8 V (Adjust)

Package Options (PTH12010x❒❒) (1)

Code	Description	Pkg Ref. (2)
AH	Horiz. T/H	(EUH)
AS	SMD, Standard (3)	(EUJ)

Notes: *(1) Add "T" to end of part number for tape and reel on SMD packages only.*
(2) Reference the applicable package reference drawing for the dimensions and PC board layout
(3) "Standard" option specifies 63/37, Sn/Pb pin solder material.

Pin Descriptions

Vin: The positive input voltage power node to the module, which is referenced to common *GND*.

Vout: The regulated positive power output with respect to the *GND* node.

GND: This is the common ground connection for the *Vin* and *Vout* power connections. It is also the 0 VDC reference for the control inputs.

Inhibit: The Inhibit pin is an open-collector/drain negative logic input that is referenced to *GND*. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the *Inhibit* control is active, the input current drawn by the regulator is significantly reduced. If the inhibit feature is not used the control pin should be left open-circuit. The module will then produce an output whenever a valid input source is applied.

Vo Adjust: A 1% resistor must be directly connected between this pin and *GND* (pin 1) to set the output voltage of the module higher than its lowest value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 1.2 V to 5.5 V for W-suffix devices, and 0.8 V to 1.8 V for L-suffix devices. The resistor value required for a given output voltage may be calculated using a formula. If left open circuit, the output voltage will default to its lowest value. For further information on output voltage adjustment consult the related application note.

The specification table gives the preferred resistor values for a number of standard output voltages.

Vo Sense: The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy *Vo Sense* should be connected to *Vout*. It can also be left disconnected.

Track: This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output will follow the voltage at the *Track* pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_{in}. *Note: Due to the under-voltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, consult the related application note.*

Margin Down: When this input is asserted to *GND*, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accomodated with a series resistor. For further information, consult the related application note.

Margin Up: When this input is asserted to *GND*, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor. For further information, consult the related application note.

Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Track Input Voltage	V_{track}		–0.3	—	V_{in} + 0.3	V
Operating Temperature Range	T_a	Over V_{in} Range	–40 (i)	—	85	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module body or pins			235 (ii)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	—	20	—	G's
Weight	—		—	5	—	grams
Flammability	—	Meets UL 94V-O				

Notes: *(i) For operation below 0 °C the external capacitors must have stable characteristics. Use either a low-ESR tantalum, Os-Con, or ceramic capacitor.*
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =12 V, V_{out} =3.3 V, C_{in}=560 µF, C_{out} =0 µF, and I_o =$I_o$max)

Characteristics	Symbols	Conditions	PTH12010W Min	Typ	Max	Units
Output Current	I_o	1.2 V ≤ V_o ≤ 5.5 V, 60 °C, 200 LFM airflow	0	—	12 (1)	A
		25 °C, natural convection	0	—	12 (1)	
Input Voltage Range	V_{in}	Over I_o range	10.8	—	13.2	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2 (2)	%V_o
Temperature Variation	ΔReg_{temp}	–40 °C <T_a < +85 °C	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±10	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±12	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_a ≤ +85 °C	—	—	±3 (2)	%V_o
Output Voltage Adjust Range	ΔV_{adj}	Over V_{in} range	1.2	—	5.5	V
Efficiency	η	I_o =8 A, R_{SET} = 280 Ω, V_o=5.0 V	—	94	—	%
		R_{SET} = 2.0 kΩ, V_o=3.3 V	—	93	—	
		R_{SET} = 4.32 kΩ, V_o=2.5 V	—	91	—	
		R_{SET} = 11.5 kΩ, V_o=1.8 V	—	89	—	
		R_{SET} = 24.3 kΩ, V_o=1.5 V	—	88	—	
		R_{SET} = open cct, V_o=1.2 V	—	86	—	
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth, V_o≤2.5 V	—	25	—	mVpp
		V_o>2.5 V	—	1	—	% V_o
Over-Current Threshold	I_o trip	Reset, followed by auto-recovery	—	20	—	A
Transient Response		1 A/µs load step, 50 to 100 % $I_o$max, C_{out} =330 µF				
	t_{tr}	Recovery Time	—	70	—	µSec
	ΔV_{tr}	V_o over/undershoot	—	100	—	mV
Margin Up/Down Adjust	V_o adj		—	± 5	—	%
Margin Input Current (pins 9 /10)	I_{IL} margin	Pin to GND	—	– 8 (3)	—	µA
Track Input Current (pin 8)	I_{IL} track	Pin to GND	—	—	–0.13 (4)	mA
Track Slew Rate Capability	dV_{track}/dt	C_{out} ≤ C_{out}(max)	—	—	1	V/ms
Under-Voltage Lockout	UVLO	V_{in} increasing	—	9.5	10.4	V
		V_{in} decreasing	8.8	9	—	
Inhibit Control (pin3)		Referenced to GND				
Input High Voltage	V_{IH}		V_{in} –0.5	—	Open (4)	V
Input Low Voltage	V_{IL}		–0.2	—	0.5	
Input Low Current	I_{IL} inhibit	Pin to GND	—	–0.24	—	mA
Input Standby Current	I_{in} inh	Inhibit (pin 3) to GND, Track (pin 8) open	—	10	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges	300	350	400	kHz
External Input Capacitance	C_{in}		560 (5)	—	—	µF
External Output Capacitance	C_{out}	Capacitance value, non-ceramic	0	330 (6)	6,600 (7)	µF
		ceramic	0	—	300	
		Equiv. series resistance (non-ceramic)	4 (8)	—	—	mΩ
Reliability	MTBF	Per Bellcore TR-332, 50 % stress, T_a =40 °C, ground benign	6.4	—	—	10^6 Hrs

Notes: *(1) See SOA curves or consult factory for appropriate derating.*

(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1 %, with 100 ppm/°C (or better) temperature stability.

(3) A small low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.

(4) This control pin has an internal pull-up to the input voltage Vin (7.5 V for pin 8). If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.

(5) A 560 µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimum of 800 mA rms of ripple current.

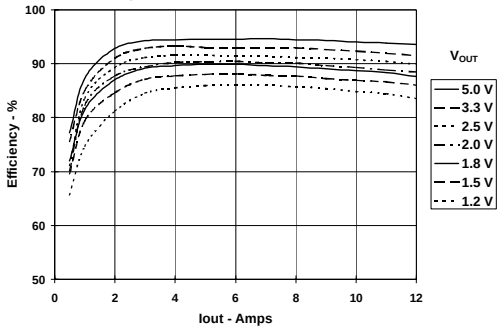
(6) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load will improve the transient response.

(7) This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult the application notes for further guidance.

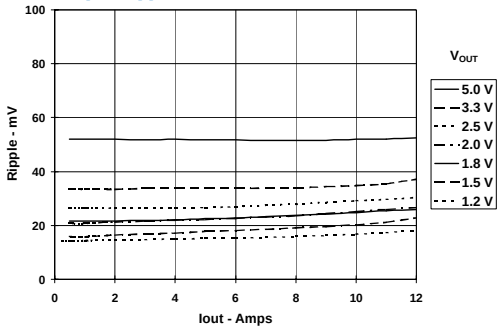
(8) This is the typical ESR for all the electrolytic (non-ceramic) ouput capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

PTH12010W Characteristic Data; V_{in} =12 V *(See Note A)*

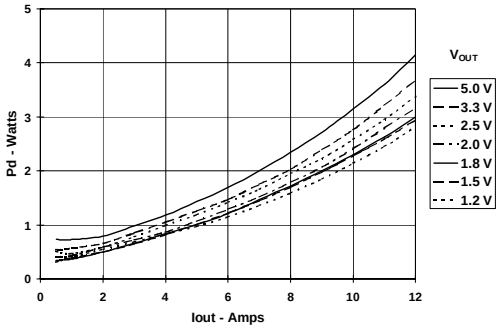
Efficiency vs Load Current



Output Ripple vs Load Current

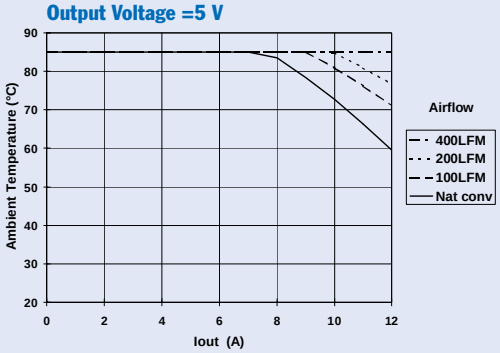


Power Dissipation vs Load Current

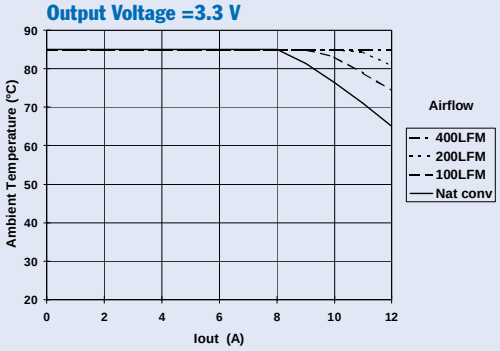


PTH12010W Safe Operating Area; V_{in} =12 V *(See Note B)*

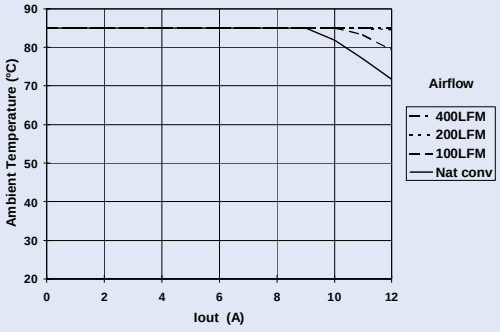
Output Voltage =5 V



Output Voltage =3.3 V



Output Voltage ≤1.8 V



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =12 V, V_{out} =1.8 V, C_{in}=560 µF, C_{out} =0 µF, and I_o =$I_o$max)

			PTH12010L			
Characteristics	**Symbols**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Output Current	I_o	0.8 V ≤ V_o ≤ 1.8 V, 60 °C, 200 LFM airflow	0	—	12 (1)	A
		25 °C, natural convection	0	—	12 (1)	
Input Voltage Range	V_{in}	Over I_o range	10.8	—	13.2	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2 (2)	%V_o
Temperature Variation	ΔReg_{temp}	–40 °C <T_a < +85 °C	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±10	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±12	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_a ≤ +85 °C	—	—	±3 (2)	%V_o
Output Voltage Adjust Range	ΔV_{adj}	Over V_{in} range	0.8	—	1.8	V
Efficiency	η	I_o =8 A, R_{SET} =130 Ω, V_o = 1.8 V	—	89	—	%
		R_{SET} = 3.57 kΩ, V_o = 1.5 V	—	88	—	
		R_{SET} = 12.1 kΩ, V_o = 1.2 V	—	86	—	
		R_{SET} = 32.4 kΩ, V_o = 1.0 V	—	84	—	
		R_{SET} = open cct, V_o = 0.8 V	—	82	—	
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth, V_o ≤ 1 V	—	25	—	mVpp
		V_o > 1 V	—	1	—	% V_o
Over-Current Threshold	I_o trip	Reset, followed by auto-recovery	—	20	—	A
Transient Response		1 A/µs load step, 50 to 100 % $I_o$max, C_{out} =330 µF				
	t_{tr}	Recovery Time	—	70	—	µSec
	ΔV_{tr}	V_o over/undershoot	—	100	—	mV
Margin Up/Down Adjust	V_o adj		—	± 5	—	%
Margin Input Current (pins 9 /10)	I_{IL} margin	Pin to GND	—	– 8 (3)	—	µA
Track Input Current (pin 8)	I_{IL} track	Pin to GND	—	—	–0.13 (4)	mA
Track Slew Rate Capability	dV_{track}/dt	C_{out} ≤ C_{out}(max)	—	—	1	V/ms
Under-Voltage Lockout	UVLO	V_{in} increasing	—	9.5	10.4	V
		V_{in} decreasing	8.8	9	—	
Inhibit Control (pin3)		Referenced to GND				
Input High Voltage	V_{IH}		V_{in} –0.5	—	Open (4)	V
Input Low Voltage	V_{IL}		–0.2	—	0.5	
Input Low Current	I_{IL} inhibit	Pin to GND	—	–0.24	—	mA
Input Standby Current	I_{in} inh	Inhibit (pin 3) to GND, Track (pin 8) open	—	10	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges	200	250	300	kHz
External Input Capacitance	C_{in}		560 (5)	—	—	µF
External Output Capacitance	C_{out}	Capacitance value, non-ceramic	0	330 (6)	6,600 (7)	µF
		ceramic	0	—	300	
		Equiv. series resistance (non-ceramic)	4 (8)	—	—	mΩ
Reliability	MTBF	Per Bellcore TR-332, 50 % stress, T_a =40 °C, ground benign	6.4	—	—	10^6 Hrs

Notes: *(1) See SOA curves or consult factory for appropriate derating.*

(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1 %, with 100 ppm/°C (or better) temperature stability.

(3) A small low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.

(4) This control pin has an internal pull-up to the input voltage Vin (7.5 V for pin 8). If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.

(5) A 560 µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimum of 800 mA rms of ripple current.

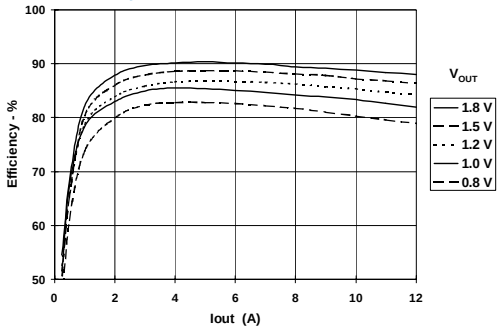
(6) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load will improve the transient response.

(7) This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult the application notes for further guidance.

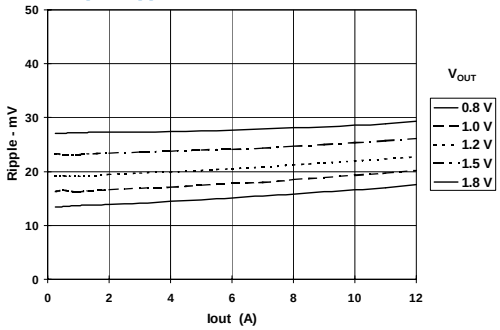
(8) This is the typical ESR for all the electrolytic (non-ceramic) ouput capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

PTH12010L Characteristic Data; V_{in} =12 V *(See Note A)*

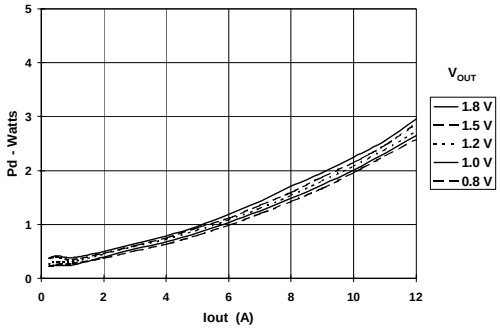
Efficiency vs Load Current



Output Ripple vs Load Current

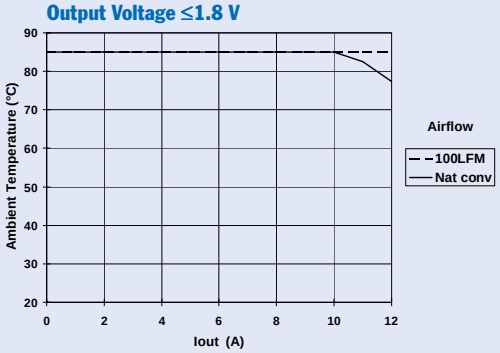


Power Dissipation vs Load Current



PTH12010L Safe Operating Area; V_{in} =12 V *(See Note B)*

Output Voltage ≤1.8 V



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

Capacitor Recommendations for the PTH12010 Series of Power Modules

Input Capacitor

The recommended input capacitance is determined by the 560 µF [1] minimum capacitance and 800 mArms minimum ripple current rating. A 10-µF X5R/X7R ceramic capacitor may also be added to reduce the reflected input ripple current. The ceramic capacitor should be located between the input electrolytic and the module.

Ripple current, less than 100 mΩ equivalent series resistance (ESR) and temperature are major considerations when selecting input capacitors. Unlike polymer-tantalum capacitors, regular tantalum capacitors have a recommended minimum voltage rating of 2 × (max. DC voltage + AC ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with sufficient voltage rating to meet this requirement. At temperatures below 0 °C, the ESR of aluminum electrolytic capacitors increases. For these applications Os-Con, polymer-tantalum, and polymer-aluminum types should be considered.

Output Capacitors (Optional)

For applications with load transients (sudden changes in load current), regulator response will benefit from external output capacitance. The value of 330 µF is used to define the transient response specification (see data sheet). For most applications, a high quality computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable for ambient temperatures above 0 °C. Below 0 °C, tantalum, ceramic or Os-Con type capacitors are recommended. When using one or more non-ceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 1-1.

In addition to electrolytic capacitance, adding a 10-µF X5R/X7R ceramic capacitor to the output will reduce the output ripple voltage and improve the regulator's transient response. The measurement of both the output ripple and transient response is also best achieved across a 10-µF ceramic capacitor.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum type capacitors are most suited for use on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0 °C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution many general purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit will be encountered well before the maximum capacitance value is reached.

Capacitor Table

Table 1-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Designing for Very Fast Load Transients

The transient response of the DC/DC converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any DC/DC converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the data sheet, or the total amount of load capacitance is above 3,000 µF, the selection of output capacitors becomes more important.

Table 1-1: Input/Output Capacitors

Capacitor Vendor, Type/ Series, (Style)	Capacitor Characteristics					Quantity		
	Working Voltage	Value (µF)	Max. ESR at 100 kHz	Max. Ripple Current at 85 °C (Irms)	Physical Size (mm)	Input Bus	Optional Output Bus	Vendor Part Number
Panasonic, Aluminum FC, (Radial) FK, (SMD)	25 V 25 V 35 V	560 1000 680	0.065 Ω 0.060 Ω 0.060 Ω	1205 mA 1100 mA 1100 mA	12.5×15 12.5×13.5 12.5×13.5	1 1 1	1 1 1	EEUFC1E561S EEVFK1E102Q EEVFK1V681Q
United Chemi-Con FX, Os-con (SMD) LXZ, Aluminum (Radial) PS, Poly-Aluminum (Radial) PXA, Poly-Aluminum (SMD	16 V 16 V 16 V 16 V	330 330 680 330	0.018 Ω 0.014 Ω 0.068 Ω 0.014 Ω	4500 mA 5050 mA 1050 mA 5050 mA	10×10.5 10×12.5 10×16 10x12.2	2 2 1 2	≤3 ≤2 1 ≤2	16FX330M 16PS330MJ12 LXZ16VB681M10X16LL PXA16VC331MJ12
Nichicon, Aluminum PM, (Radial) HD, (Radial)	25 V 16 V 35 V	560 680 560	0.060 Ω 0.038 Ω 0.048 Ω	1060 mA 1430 mA 1360 mA	12.5×15 10×16 16×15	1 1 1	1 1 1	UPM1E561MHH6 UHD1C681MHR UPM1V561MHH6
Panasonic, Poly-Aluminum: WA, (SMD) S/SE, (SMD)	16 V 6.3 V	330 180	0.022 Ω 0.005 Ω	4100 mA 4000 mA	10×10.2 7.3×4.3×4.2	2 N/R [2]	≤3 ≤1 [3]	EEFWA1C331P EEFSE0J181R **(V_o ≤5.1V)**
Sanyo TPE Poscap (SMD) SP, Os-Con (Radial) SVP, Os-Con (SMD)	10 V 16 V 16 V	330 270 330	0.025 Ω 0.018 Ω 0.016 Ω	3000 mA >3500 mA 4700 mA	7.3L ×5.7W 10×10.5 11×12	N/R [2] 2 [1] 2	≤4 ≤3 ≤3	10TPE330M 16SP270M 16SVP330M
AVX, Tantalum Series III TPS (SMD)	10 V 10 V	470 330	0.045 Ω 0.045 Ω	>1723 mA >1723 mA	7.3L ×5.7W ×4.1H	N/R [2] N/R [2]	≤5 [3] ≤5 [3]	TPSE477M010R0045 **(V_o ≤5.1V)** TPSE337M010R0045 **(V_o ≤5.1V)**
Kemet T520, Poly-Tantalum (SMD) T530, Poly-Tant/Organic	10 V 10 V 6.3 V	330 330 470	0.040 Ω 0.015 Ω 0.012 Ω	1800 mA >3800 mA 4200 mA	4.3W ×7.3L ×4.0H	N/R [2] N/R [2] N/R [2]	≤5 ≤2 ≤2 [3]	T520X337M010AS T530X337M010AS T530X477M006AS **(V_o ≤5.1V)**
Vishay-Sprague 595D, Tantalum (SMD) 94SP, Os-con (Radial)	10 V 16 V	470 270	0.100 Ω 0.018 Ω	1440 mA 4200 mA	7.2L×6W ×4.1H 10x10.5	N/R [2] 2 [1]	≤5 [3] ≤3	595D477X0010R2T **(V_o ≤5.1V)** 94SP277X0016FBP
Kemet, Ceramic X5R (SMD)	16 V 6.3 V	10 47	0.002 Ω 0.002 Ω	—	1210 case 3225 mm	1 [4] N/R [2]	≤5 ≤5	C1210C106M4PAC C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3 V 6.3 V 16 V 16 V	100 47 22 10	0.002 Ω	—	1210 case 3225 mm	N/R [2] N/R [2] 1 [4] 1 [4]	≤3 ≤5 ≤5 ≤5	GRM32ER60J107M GRM32ER60J476M GRM32ER61C226K GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 V 6.3 V 16 V 16 V	100 47 22 10	0.002 Ω	—	1210 case 3225 mm	N/R [2] N/R [2] 1 [4] 1 [4]	≤3 ≤5 ≤5 ≤5	C3225X5R0J107MT C3225X5R0J476MT C3225X5R1C226MT C3225X5R1C106MT

[1] A total capacitance of 540 µF is acceptable based on the combined ripple current rating.
[2] N/R –Not recommended. The capacitor voltage rating does not meet the minimum derated operating limits.
[3] The voltage rating of this capacitor only allows it to be used for output voltages that are equal to or less than 5.1 V.
[4] A ceramic capacitor may be used to complement electrolytic types at the input to further reduce high-frequency ripple current.

Adjusting the Output Voltage of the PTH12010x Series of Wide-Output Adjust Power Modules

The *V_o Adjust* control (pin 4) sets the output voltage of the PTH12010 product. The adjustment range is from 1.2 V to 5.5 V for the W-suffix modules, and 0.8 V to 1.8 V for L-suffix modules. The adjustment method requires the addition of a single external resistor, R_{set}, that must be connected directly between the *V_o Adjust* and *GND* pins [1]. Table 2-1 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides. Figure 2-1 shows the placement of the required resistor.

Table 2-1; Preferred Values of R_{set} for Standard Output Voltages

	PTH12010W		PTH12010L	
V_{out} (Req'd)	**R_{set}**	**V_{out} (Actual)**	**R_{set}**	**V_{out} (Actual)**
5 V	280 Ω	5.009 V	N/A	N/A
3.3 V	2.0 kΩ	3.294 V	N/A	N/A
2.5 V	4.32 kΩ	2.503 V	N/A	N/A
2 V	8.06 kΩ	2.010 V	N/A	N/A
1.8 V	11.5 kΩ	1.801 V	130 Ω	1.800 V
1.5 V	24.3 kΩ	1.506 V	3.57 kΩ	1.499 V
1.2 V	Open	1.200 V	12.1 kΩ	1.201 V
1.1 V	N/A	N/A	18.7 kΩ	1.101 V
1.0 V	N/A	N/A	32.4 kΩ	0.999 V
0.9 V	N/A	N/A	71.5 kΩ	0.901 V
0.8 V	N/A	N/A	Open	0.800 V

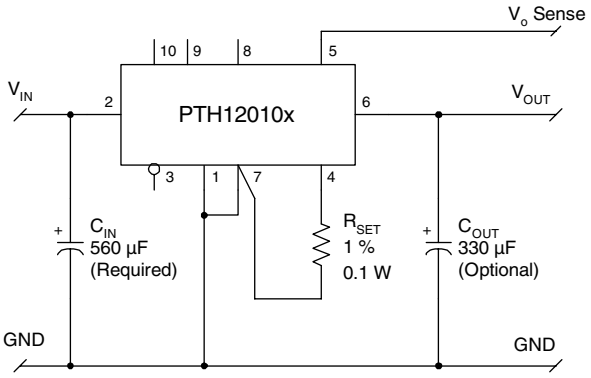
For other output voltages the value of the required resistor can either be calculated, or simply selected from the range of values given in Table 2-3. The following formula may be used for calculating the adjust resistor value. Select the appropriate value for the parameters, R_s and V_{min}, from Table 2.2.

$$R_{set} = 10\ k\Omega \cdot \frac{0.8\ V}{V_{out} - V_{min}} - R_s \quad k\Omega$$

Table 2.2; Adjust Formula Parameters

Pt. No.	PTH12010W	PTH12010L
V_{min}	1.2 V	0.8 V
V_{max}	5.5 V	1.8 V
R_s	1.82 kΩ	7.87 kΩ

Figure 2-1; V_o Adjust Resistor Placement



Notes:

1. A 0.05 W rated resistor may be used. The tolerance should be 1 %, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.
2. Never connect capacitors from *V_o Adjust* to either *GND* or *V_{out}*. Any capacitance added to the *V_o Adjust* pin will affect the stability of the regulator.

Table 2-3; Output Voltage Set-Point Resistor Values

PTH12010W				PTH12010L	
V_{OUT}	R_{SET}	V_{OUT}	R_{SET}	V_{OUT}	R_{SET}
1.200	Open	2.70	3.51 kΩ	0.800	Open
1.225	318.0 kΩ	2.75	3.34 kΩ	0.825	312.0 kΩ
1.250	158.0 kΩ	2.80	3.18 kΩ	0.850	152.0 kΩ
1.275	105.0 kΩ	2.85	3.03 kΩ	0.875	98.8 kΩ
1.300	78.2 kΩ	2.90	2.89 kΩ	0.900	72.1 kΩ
1.325	62.2 kΩ	2.95	2.75 kΩ	0.925	56.1 kΩ
1.350	51.5 kΩ	3.00	2.62 kΩ	0.950	45.5 kΩ
1.375	43.9 kΩ	3.05	2.50 kΩ	0.975	37.8 kΩ
1.400	38.2 kΩ	3.10	2.39 kΩ	1.000	32.1 kΩ
1.425	33.7 kΩ	3.15	2.28 kΩ	1.025	27.7 kΩ
1.450	30.2 kΩ	3.20	2.18 kΩ	1.050	24.1 kΩ
1.475	27.3 kΩ	3.25	2.08 kΩ	1.075	21.2 kΩ
1.50	24.8 kΩ	3.30	1.99 kΩ	1.100	18.8 kΩ
1.55	21.0 kΩ	3.35	1.90 kΩ	1.125	16.7 kΩ
1.60	18.2 kΩ	3.40	1.82 kΩ	1.150	15.0 kΩ
1.65	16.0 kΩ	3.50	1.66 kΩ	1.175	13.5 kΩ
1.70	14.2 kΩ	3.60	1.51 kΩ	1.200	12.1 kΩ
1.75	12.7 kΩ	3.70	1.38 kΩ	1.225	11.0 kΩ
1.80	11.5 kΩ	3.80	1.26 kΩ	1.250	9.91 kΩ
1.85	10.5 kΩ	3.90	1.14 kΩ	1.275	8.97 kΩ
1.90	9.61 kΩ	4.00	1.04 kΩ	1.300	8.13 kΩ
1.95	8.85 kΩ	4.10	939 Ω	1.325	7.37 kΩ
2.00	8.18 kΩ	4.20	847 Ω	1.350	6.68 kΩ
2.05	7.59 kΩ	4.30	761 Ω	1.375	6.04 kΩ
2.10	7.07 kΩ	4.40	680 Ω	1.400	5.46 kΩ
2.15	6.60 kΩ	4.50	604 Ω	1.425	4.93 kΩ
2.20	6.18 kΩ	4.60	533 Ω	1.450	4.44 kΩ
2.25	5.80 kΩ	4.70	466 Ω	1.475	3.98 kΩ
2.30	5.45 kΩ	4.80	402 Ω	1.50	3.56 kΩ
2.35	5.14 kΩ	4.90	342 Ω	1.55	2.8 kΩ
2.40	4.85 kΩ	5.00	285 Ω	1.60	2.13 kΩ
2.45	4.58 kΩ	5.10	231 Ω	1.65	1.54 kΩ
2.50	4.33 kΩ	5.20	180 Ω	1.70	1.02 kΩ
2.55	4.11 kΩ	5.30	131 Ω	1.75	551 Ω
2.60	3.89 kΩ	5.40	85 Ω	1.80	130 Ω
2.65	3.70 kΩ	5.50	41 Ω		

Features of the PTH Family of Non-Isolated Wide Output Adjust Power Modules

POLA™ Compatibility

The PTH/PTV family of non-isolated, wide-output adjustable power modules from Texas Instruments are optimized for applications that require a flexible, high performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, non-isolated modules with the same footprint and form factor. POLA parts are also assured to be interoperable, thereby providing customers with true second-source availability.

From the basic, "Just Plug it In" functionality of the 6-A modules, to the 30-A rated feature-rich PTHxx030, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 3-1 provides a quick reference to the features by product series and input bus voltage.

Table 3-1; Operating Features by Series and Input Bus Voltage

Series	Input Bus	I_{OUT}	Adjust (Trim)	On/Off Inhibit	Over-Current	Pre-Bias Startup	Auto-Track™	Margin Up/Down	Output Sense	Thermal Shutdown
PTHxx050	3.3 V	6 A	•	•	•	•	•			
	5 V	6 A	•	•	•	•	•			
	12 V	6 A	•	•	•	•	•			
PTHxx060	3.3 V / 5 V	10 A	•	•	•	•	•	•	•	
	12 V	8 A	•	•	•	•	•	•	•	
PTHxx010	3.3 V / 5 V	15 A	•	•	•	•	•	•	•	
	12 V	12 A	•	•	•	•	•	•	•	
PTVxx010	5 V	8 A	•	•	•	•	•		•	
	12 V	8 A	•	•	•	•	•		•	
PTHxx020	3.3 V / 5 V	22 A	•	•	•	•	•	•	•	•
	12 V	18 A	•	•	•	•	•	•	•	•
PTVxx020	5 V	18 A	•	•	•	•	•		•	•
	12 V	16 A	•	•	•	•	•		•	•
PTHxx030	3.3 V / 5 V	30 A	•	•	•	•	•	•	•	•
	12 V	26 A	•	•	•	•	•	•	•	•

For simple point-of-use applications, the PTH12050 (6 A) provides operating features such as an on/off inhibit, output voltage trim, pre-bias start-up and over-current protection. The PTH12060 (10 A), and PTH12010 (12 A) include an output voltage sense, and margin up/down controls. Then the higher output current, PTH12020 (18 A) and PTH12030 (26 A) products incorporate over-temperature shutdown protection.

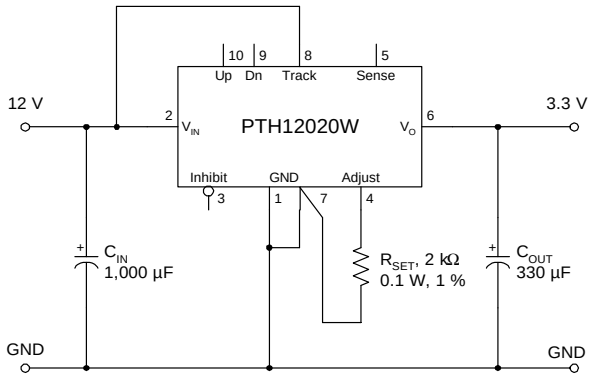
The PTV12010 and PTV12020 are similar parts offered in a vertical, single in-line pin (SIP) profile, at slightly lower current ratings.

All of the products referenced in Table 3-1 include Auto-Track™. This feature was specifically designed to simplify the task of sequencing the supply voltages in a power system. This and other features are described in the following sections.

Soft-Start Power Up

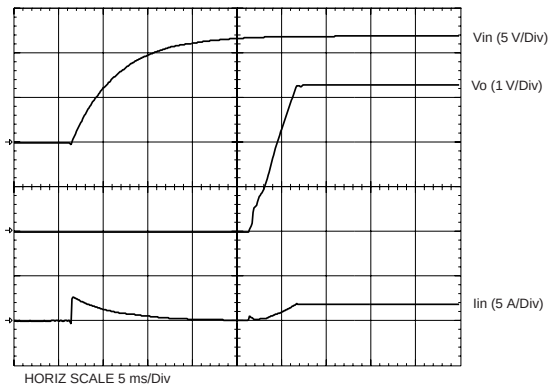
The Auto-Track feature allows the power-up of multiple PTH modules to be directly controlled from the *Track* pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the *Track* pin should be directly connected to the input voltage, V_{in} (see Figure 3-1).

Figure 3–1



When the *Track* pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

Figure 3–2



From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8 ms-15 ms) before allowing the output voltage to rise. The output then progressively rises to the module's set-point voltage. Figure 3-2 shows the soft-start power-up characteristic of the 18-A output product (PTH12020W), operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 25 ms.

Over-Current Protection

For protection against load faults, all modules incorporate output over-current protection. Applying a load that exceeds the regulator's over-current threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Over-Temperature Protection (OTP)

The PTH12020W and PTH12030W products have over-temperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's *Inhibit* control is internally pulled low. This turns the output off. The output voltage will drop as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

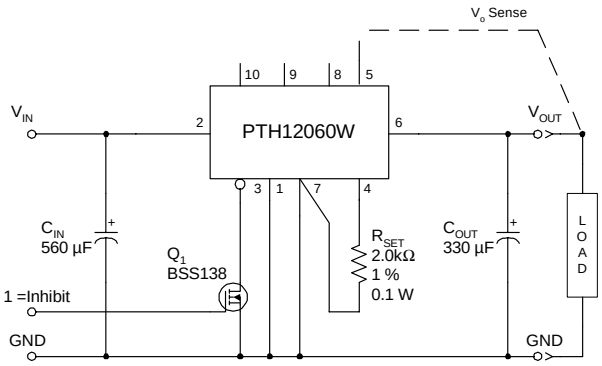
Output On/Off Inhibit

For applications requiring output voltage on/off control, each series of the PTH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_{in} with respect to *GND*.

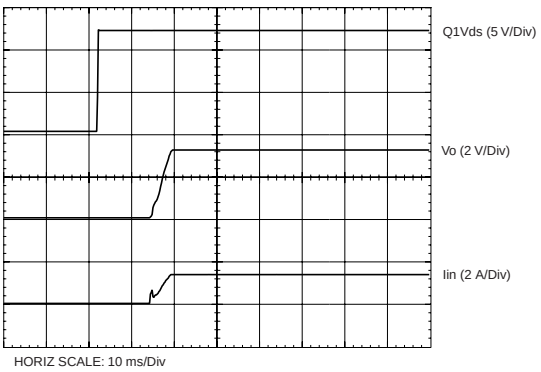
Figure 3-3 shows the typical application of the inhibit function. Note the discrete transistor (Q_1). The *Inhibit* input has its own internal pull-up to a potential of 5 V to 13.2 V (see footnotes to specification table). The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

Figure 3–3



Turning Q_1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q_1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 25 msec. Figure 3-4 shows the typical rise in both the output voltage and input current, following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, Q_1 V_{ds}. The waveforms were measured with a 5-A constant current load.

Figure 3–4



Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

How Auto-Track Works

Auto-Track works by forcing the module's output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set-point [1]. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its Track pin on a volt-for-volt basis. By connecting the Track pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit [3]. For convenience the Track control incorporates an internal RC charge circuit. This operates off the module's input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q_1 in Figure 3-5.

To initiate a power-up sequence, it is recommended that the Track control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic-level high signal to the circuit's On/Off Control turns Q_1 on and applies a ground signal to the Track pins. After completing their internal soft-start intialization, the output of all modules will remain at zero volts while Q_1 is on.

10 ms after a valid input voltage has been applied to the modules, Q_1 may be turned off. This allows the track control voltage to automatically rise toward to the modules' input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 3-6 shows the output voltage waveforms from the circuit of Figure 3-5 after the On/Off Control is set from a high to a low-level voltage. The waveforms, Vo_1 and Vo_2 represent the output voltages from the two power modules, U_1 (3.3 V) and U_2 (2 V) respectively. Vo_1 and Vo_2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q_1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track's slew rate capability, which is 1 V/ms. The components R_1 and C_1 in Figure 3-5 limit the rate at which Q_1 can pull down the Track control voltage. The values of 100 k-ohm and 0.1 µF correlate to a decay rate of about 0.17 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 3-7 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track control.

Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absloute maximum voltage that may be applied to the Track pin is the input voltage V_{in}.
4. The module will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the Track pin be held at ground potential.
5. The module is capable of both sinking and sourcing current when following a voltage at its Track pin. Therefore startup into an output prebias cannot be supported when a module is under Auto-Track control. *Note: A pre-bias holdoff is not necessary when all supply voltages rise simultaneously under the control of Auto-Track.*
6. The Auto-Track function can be disabled by connecting the *Track* pin to the input voltage (V_{in}). When Auto-Track is disabled, the output voltage will rise at a quicker and more linear rate after input power is applied.

Figure 3–5; Sequenced Power Up & Power Down Using Auto-Track

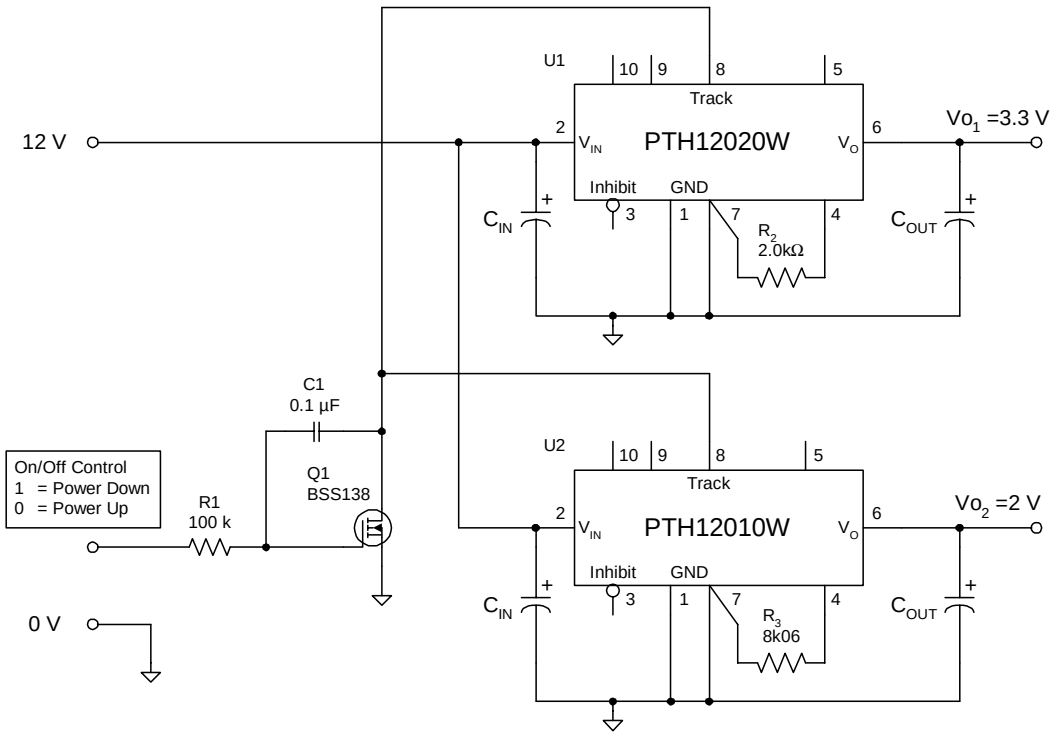


Figure 3–6; Simultaneous Power Up with Auto-Track Control

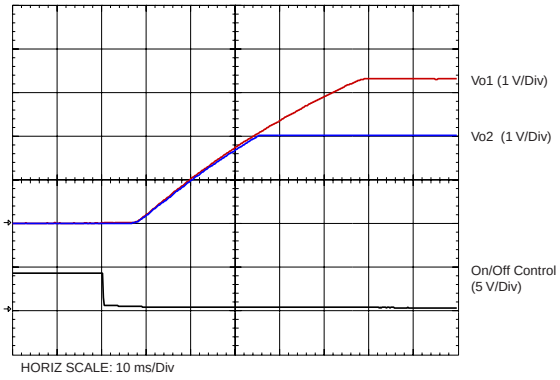
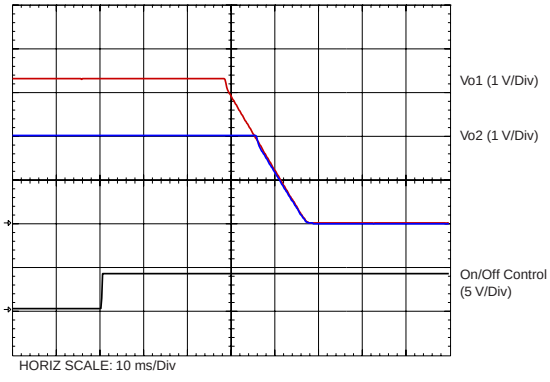


Figure 3–7; Simultaneous Power Down with Auto-Track Control



Margin Up/Down Controls

The PTH12060, PTH12010, PTH12020, and PTH12030 products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted [1], either up or down, by a nominal 5%. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5% change is applied to the adjusted output voltage, as set by the external resistor, R_{set} at the *V_o Adjust* pin.

The 5 % adjustment is made by pulling the appropriate margin control input directly to the *GND* terminal [2]. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose [3]. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs. The value of the resistor can be selected from Table 3-2, or calculated using the following formula.

Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to a value less than 5%, series resistors are required (See R_D and R_U in Figure 3-8). For the same amount of adjustment, the resistor value calculated for R_U and R_D will be the same. The formula is as follows.

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad k\Omega$$

Where $\Delta\%$ = The desired amount of margin adjust in percent.

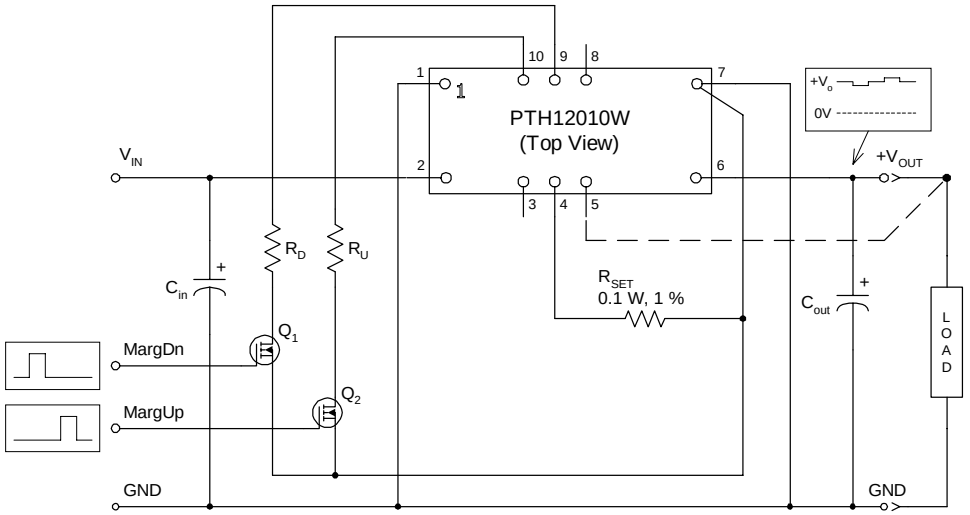
Notes:

1. The *Margin Up** and *Margin Dn** controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module *GND* at pin 7 (pin 1 for the PTHxx050). This will produce a more accurate adjustment at the load circuit terminals. The transistors Q_1 and Q_2 should be located close to the regulator.
3. The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

Table 3-2; Margin Up/Down Resistor Values

% Adjust	R_U / R_D
5	0.0 kΩ
4	24.9 kΩ
3	66.5 kΩ
2	150.0 kΩ
1	397.0 kΩ

Figure 3–8; Margin Up/Down Application Schematic



Pre-Bias Startup Capability

The capability to start up into an output pre-bias condition is now available to all the 12-V input, PTH series of power modules. (Note that this is a feature enhancement for the many of the W-suffix products) [1].

A pre-bias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The 12-V input PTH modules all incorporate synchronous rectifiers, but will not sink current during startup, or whenever the *Inhibit* pin is held low. Startup includes an initial delay (approx. 8 - 15 ms), followed by the rise of the output voltage under the control of the module's internal soft-start mechanism; see Figure 3-9.

Conditions for Pre-Bias Holdoff

In order for the module to allow an output pre-bias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a pre-bias voltage when the *Inhibit* pin is held low, and whenver the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the *Inhibit* pin (with input voltage applied), or when input power is applied with Auto-Track disabled [2]. To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its *Inhibit*), the input voltage must always be greater than the applied pre-bias source. This condition must exist throughout the power-up sequence [3].

The soft-start period is complete when the output begins rising above the pre-bias voltage. Once it is complete the module functions as normal, and will sink current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a pre-bias condition is not present, the soft-start period will be complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module's Track control pin, whichever is lowest.

Demonstration Circuit

Figure 3-10 shows the startup waveforms for the demonstration circuit shown in Figure 3-11. The initial rise in Vo_2 is the pre-bias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12010L module (Io_2) is negligible until its output voltage rises above the applied pre-bias.

Figure 3-9; PTH12020W Startup

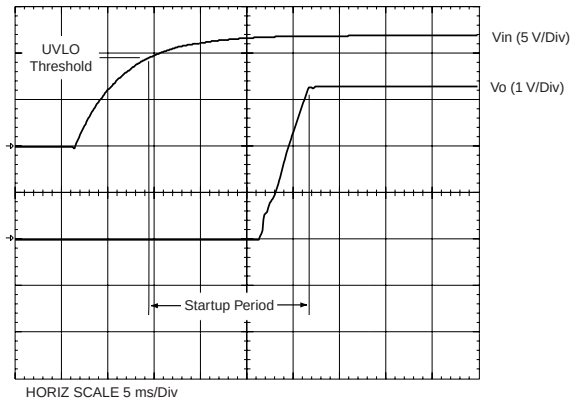
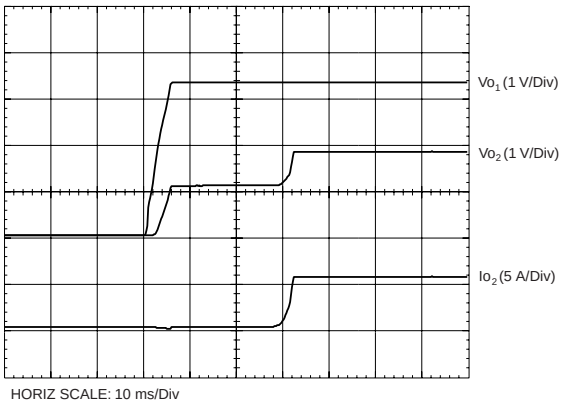


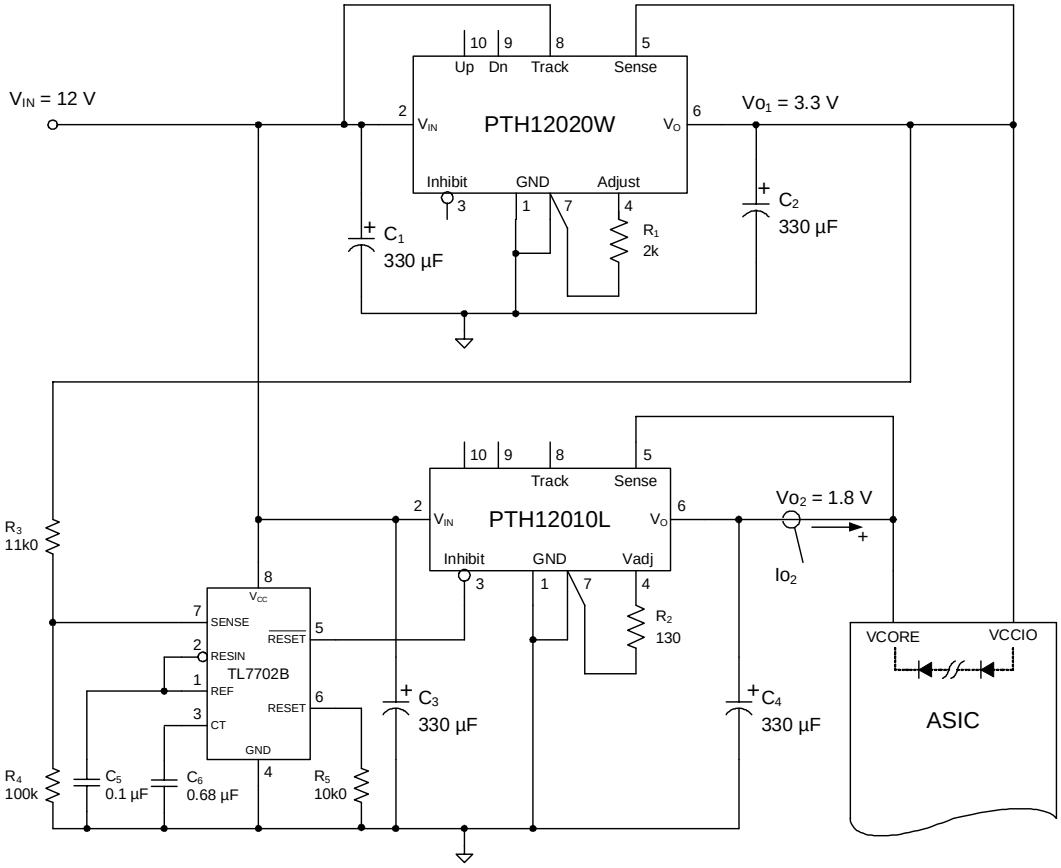
Figure 3–10; Pre-Bias Startup Waveforms



Notes

1. Output pre-bias holdoff is an inherent feature to all PTH120x0L and PTV120x0W/L modules. It has now been incorporated into all modules (including W-suffix modules with part numbers of the form PTH120x0W), with a production lot date code of "0423" or later.
2. The pre-bias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the *Track* control pin, the output will sink current during the period that the track control voltage is below that of the back-feeding source. For this reason, it is recommended that Auto-Track be disabled when not being used. This is accomplished by connecting the *Track* pin to the input voltage, Vin. This raises the *Track* pin voltage well above the set-point voltage prior to the module's start up, thereby defeating the Auto-Track feature.
3. To further ensure that the regulator's output does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage must always be greater than the applied pre-bias source. This condition must exist throughout the power-up sequence of the power system.

Figure 3–11; Application Circuit Demonstrating Pre-Bias Startup



Remote Sense

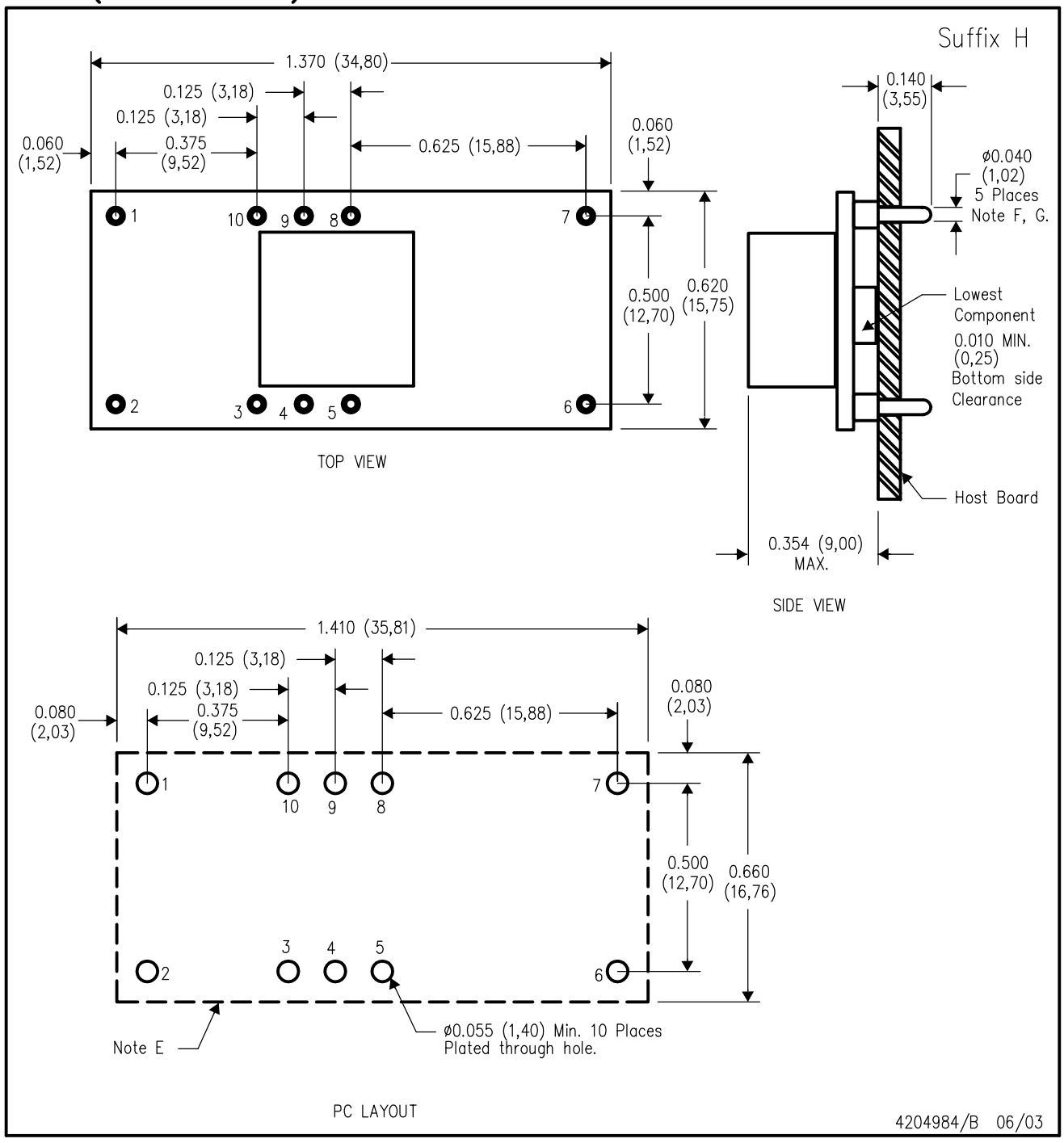
Products with this feature incorporate an output voltage sense pin, *V_o Sense*. A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between its output and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance.

To use this feature simply connect the *V_o Sense* pin to the V_{out} node, close to the load circuit (see data sheet standard application). If a sense pin is left open-circuit, an internal low-value resistor (15-Ω or less) connected between the pin and and the output node, ensures the output remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_{out} and *GND* pins, and that measured from *V_o Sense* to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

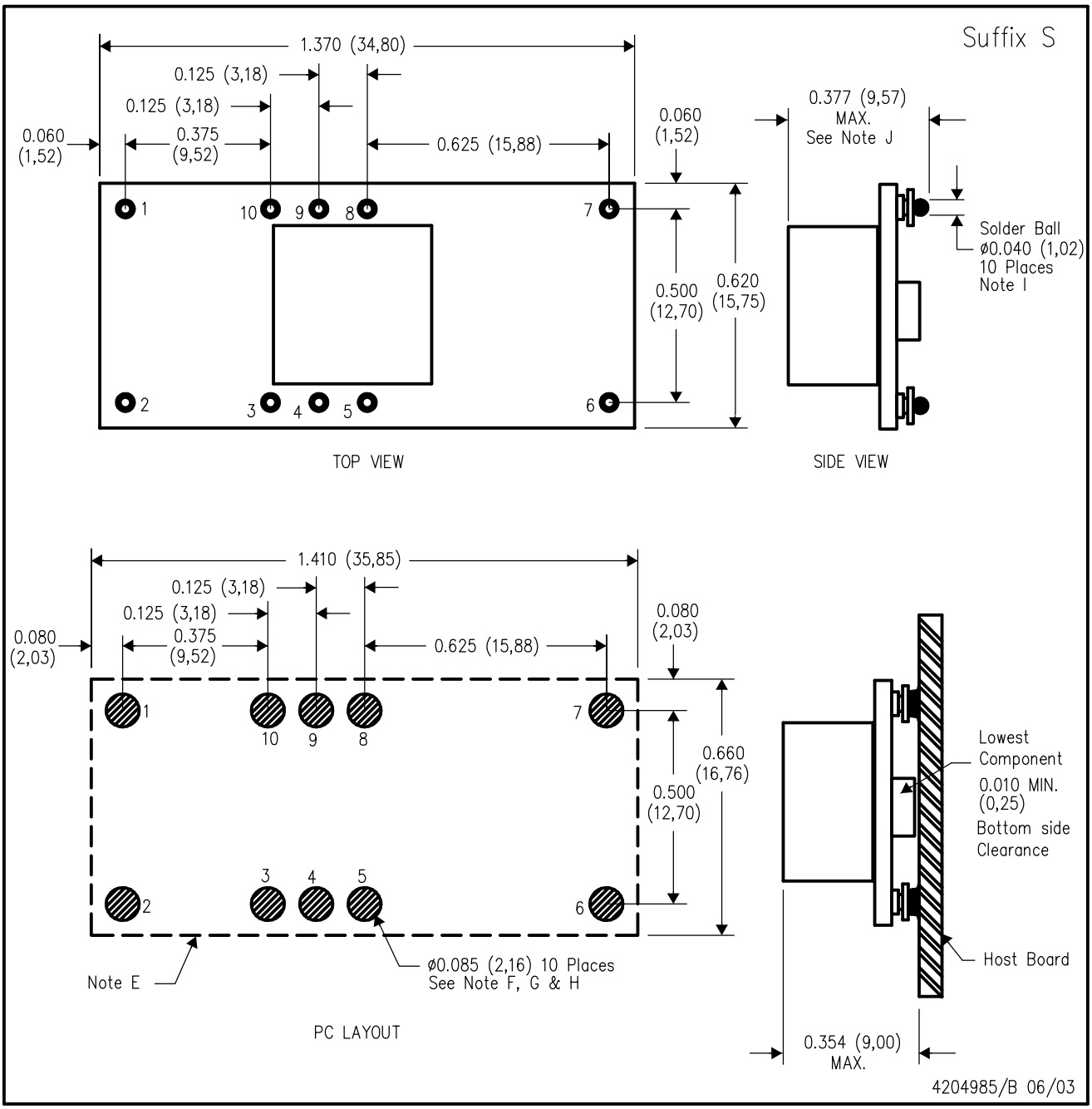
EUH (R–PDSS–T10) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EUJ (R–PDSS–B10)

DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

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