USB Function Controller

- USB specification 2.0 compliant
- Full-speed (12 Mbps) or low-speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for either full-speed or low-speed operation
- Supports two fixed-function endpoints
- Dedicated 256 byte USB buffer memory
- Integrated transceiver; no external resistors required

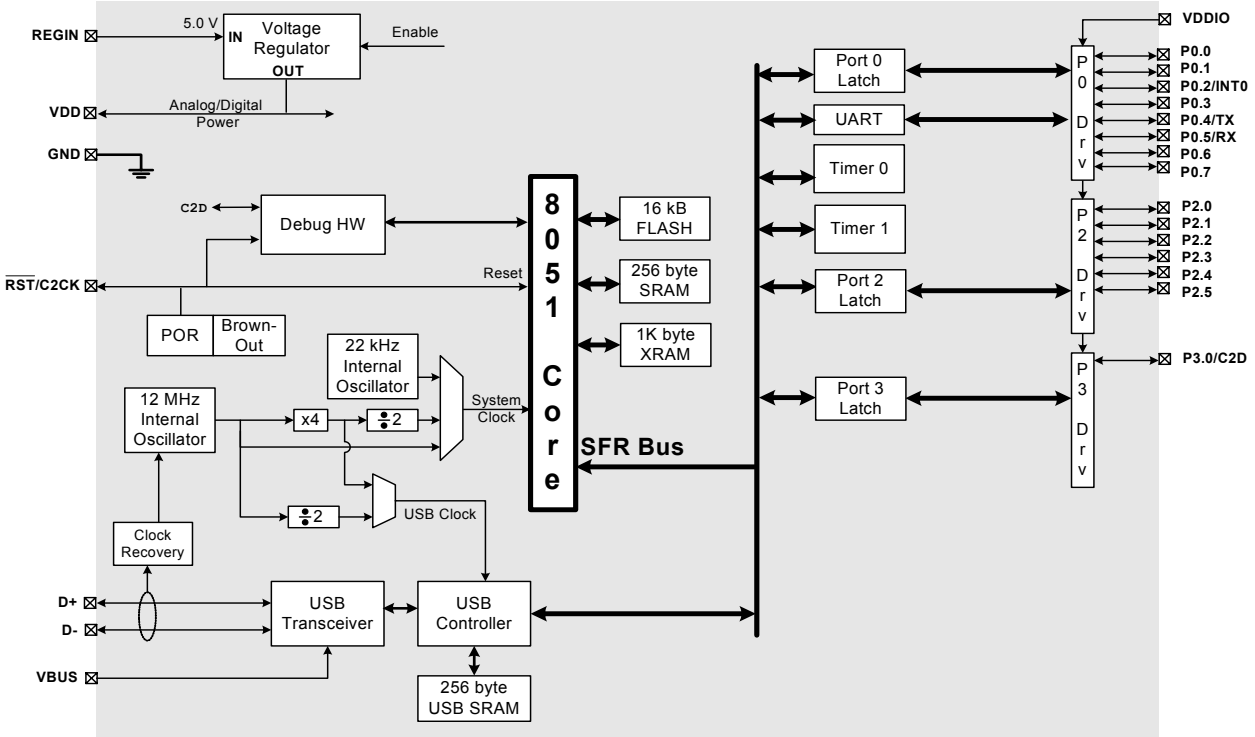
POR/Brown-Out Detector

On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping
- Inspect/modify memory, registers, and USB memory
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Separate I/O Supply Pin (V_{DDIO})

- Enables interfacing to external logic that operates between 2.0 V and V

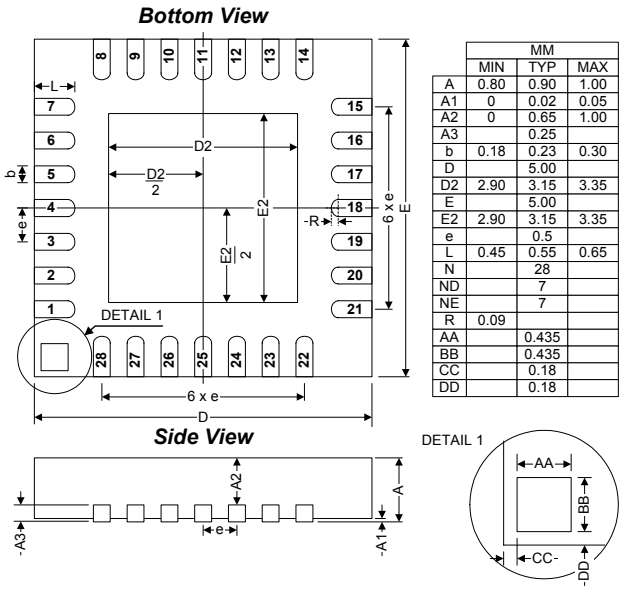


Selected Electrical Speci ications

(T_A = 40 to +70 C°, VREG = 5.0 V unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Global Characteristics					
Regulator Input Voltage (REGIN)		4.0	—	5.25	V
V_{DD} (V_{REG} Output)		3.0	3.3	3.6	V
V_{REG} Bias Current	V_{REG} Enabled	—	75	—	µA
Supply Current with CPU and USB active	CPU Clock=24 MHz, USB Clock=48 MHz CPU Clock=12 MHz, USB Clock=6 MHz	—	18 9	—	mA mA
Supply Current (suspend mode, oscillator off)	V_{DD} Monitor Enabled; V_{REG} Disabled V_{DD} Monitor Disabled; V_{REG} Disabled	—	30 <0.1	—	µA µA
CPU System Clock Range		DC	—	25	MHz
Internal Oscillator and Clocks					
Frequency	Clock Recovery Enabled Clock Recovery Disabled	11.97 11.82	12.0 12.0	12.03 12.18	MHz MHz
USB Clock	Full-Speed Operation Low-Speed Operation	47.88 5.91	48.0 6.0	48.12 6.09	MHz MHz

Package In ormation



	MM		
	MIN	TYP	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D		5.00	
D2	2.90	3.15	3.35
E		5.00	
E2	2.90	3.15	3.35
e		0.5	
L	0.45	0.55	0.65
N		28	
ND		7	
NE		7	
R	0.09		
AA		0.435	
BB		0.435	
CC		0.18	
DD		0.18	

C8051F326DK Development Kit