19-1194; Rev 2; 10/98

EVALUATION KIT AVAILABLE

+2.7V, Low-Power, Multichannel, Serial 8-Bit ADCs

General Description

The MAX1110/MAX1111 are low-power, 8-bit, 8-channel analog-to-digital converters (ADCs) that feature an internal track/hold, voltage reference, clock, and serial interface. They operate from a single +2.7V to +5.5V supply and consume only 85µA while sampling at rates up to 50ksps. The MAX1110's 8 analog inputs and the MAX1111's 4 analog inputs are software-configurable, allowing unipolar/bipolar and single-ended/differential operation.

Successive-approximation conversions are performed using either the internal clock or an external serial-interface clock. The full-scale analog input range is determined by the 2.048V internal reference, or by an externally applied reference ranging from 1V to V_{DD}. The 4-wire serial interface is compatible with the SPI™, QSPI™, and MICROWIRE™ serial-interface standards. A serial-strobe output provides the end-of-conversion signal for interrupt-driven processors.

The MAX1110/MAX1111 have a software-programmable, 2µA automatic power-down mode to minimize power consumption. Using power-down, the supply current is reduced to 6µA at 1ksps, and only 52µA at 10ksps. Power-down can also be controlled using the $\overline{SHDN}$ input pin. Accessing the serial interface automatically powers up the device.

The MAX1110 is available in 20-pin SSOP and DIP packages. The MAX1111 is available in small 16-pin QSOP and DIP packages.

Applications

- Portable Data Logging
- Hand-Held Measurement Devices
- Medical Instruments
- System Diagnostics
- Solar-Powered Remote Systems
- 4–20mA-Powered Remote Data-Acquisition Systems

Pin Configurations appear at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **+2.7V to +5.5V Single Supply**
- **Low Power: 85µA at 50ksps**
  6µA at 1ksps
- **8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1110)**
- **4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1111)**
- **Internal Track/Hold; 50kHz Sampling Rate**
- **Internal 2.048V Reference**
- **SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **Total Unadjusted Error: ±1LSB max**
  ±0.3LSB typ

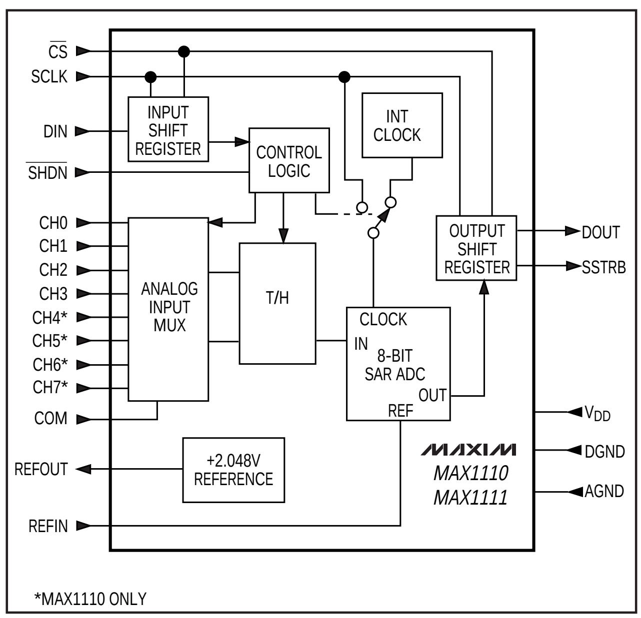
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1110CPP	0°C to +70°C	20 Plastic DIP
MAX1110CAP	0°C to +70°C	20 SSOP
MAX1110C/D	0°C to +70°C	Dice*

**Dice are specified at T_A = +25°C, DC parameters only.*

Ordering Information continued at end of data sheet.

Functional Diagram



+2.7V, Low-Power, Multichannel, Serial 8-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ....-0.3V to 6V
AGND to DGND ....-0.3V to 0.3V
CH0–CH7, COM, REFIN,
REFOUT to AGND ....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ....-0.3V to 6V
Digital Outputs to DGND...........................-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16 Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16 QSOP (derate 8.30mW/°C above +70°C)................667mW
16 CERDIP (derate 10.00mW/°C above +70°C) 800mW
20 Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20 SSOP (derate 8.00mW/°C above +70°C) 640mW
20 CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX1110C_P/MAX1111C_E...............................0°C to +70°C
MAX1110E_P/MAX1111E_E ....-40°C to +85°C
MAX1110MJP/MAX1111MJE..........................-55°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy (Note 1)	INL	V_{DD} = 2.7V to 3.6V		±0.15	±0.5	LSB
		V_{DD} = 5.5V (Note 2)		±0.2		
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		V_{DD} = 2.7V to 3.6V		±0.35	±1	LSB
		V_{DD} = 5.5V (Note 2)		±0.5		
Gain Error (Note 3)		Internal or external reference			±1	LSB
Gain Temperature Coefficient		External reference, 2.048V		±0.8		ppm/°C
Total Unadjusted Error	TUE			±0.3	±1	LSB
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (10.034kHz sine-wave input, 2.048Vp-p, 50ksps, 500kHz external clock)						
Signal-to-Noise and Distortion Ratio	SINAD			49		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			68		dB
Channel-to-Channel Crosstalk		$V_{CH\_}$ = 2.048Vp-p, 25kHz (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		1.5		MHz
Full-Power Bandwidth				800		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

	CONDITIONS		
	External clock, 2MHz		
	(Note 6)		
	Used for data transfer only		
			V
	On/off-leakage current, $V_{CH\_}$ = 0V or V_{DD}		
		3.5	mA
		±50	ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

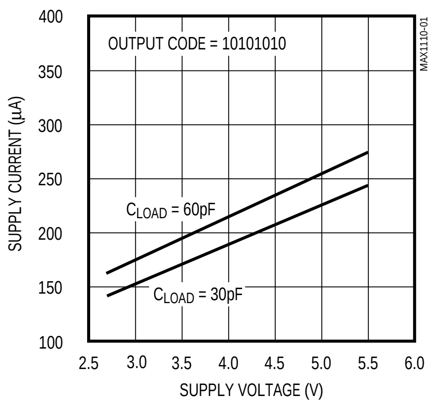
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS: DIN, SCLK, $\overline{CS}$						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \leq 3.6V$	2			V
		V_{DD} > 3.6V	3			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	Digital inputs = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ INPUT						
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid-Voltage	V_{SM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		V_{DD} / 2		V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.4	V
$\overline{SHDN}$ Input Current		$\overline{SHDN}$ = 0V or V_{DD}			±4	µA
$\overline{SHDN}$ Maximum Allowed Leakage for Mid-Input		$\overline{SHDN}$ = open			±100	nA
DIGITAL OUTPUTS: DOUT, SSTRB						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 6)			15	pF

+2.7V, Low-Power, Multichannel, Serial 8-Bit ADCs

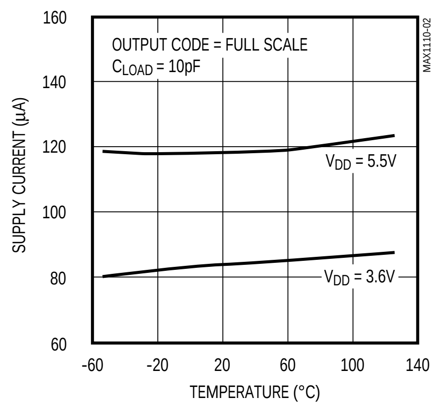
Typical Operating Characteristics

(V_{DD} = +2.7V; f_{SCLK} = 500kHz; external clock (50% duty cycle); R_L = ∞; T_A = +25°C, unless otherwise noted.)

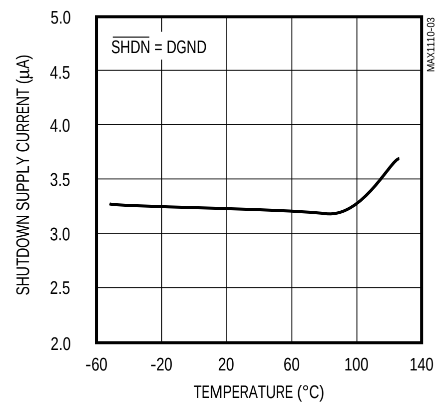
SUPPLY CURRENT vs. SUPPLY VOLTAGE



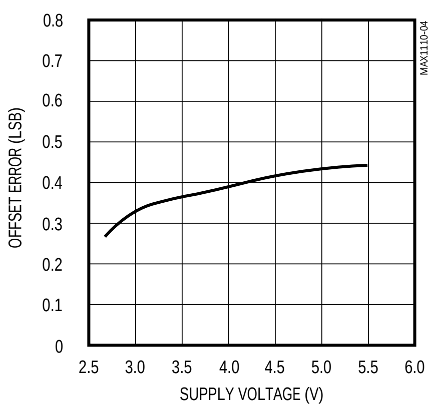
SUPPLY CURRENT vs. TEMPERATURE



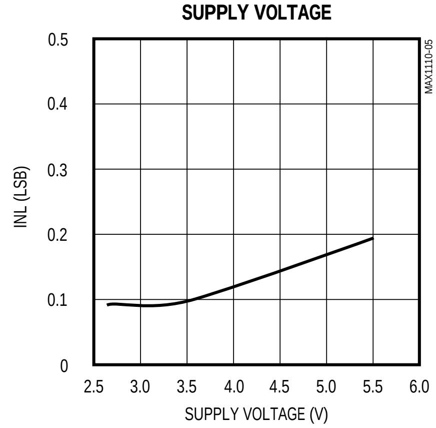
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



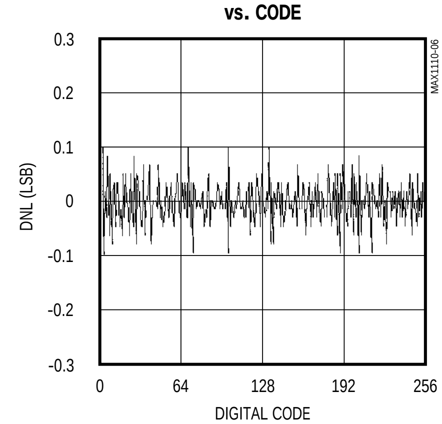
OFFSET ERROR vs. SUPPLY VOLTAGE



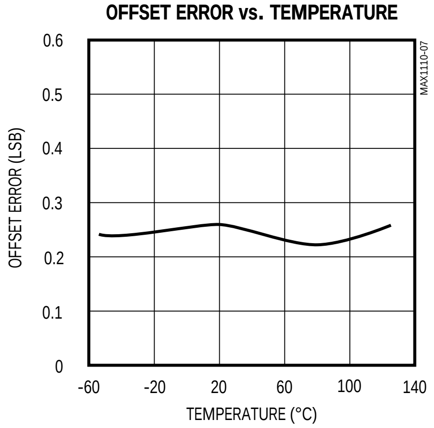
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



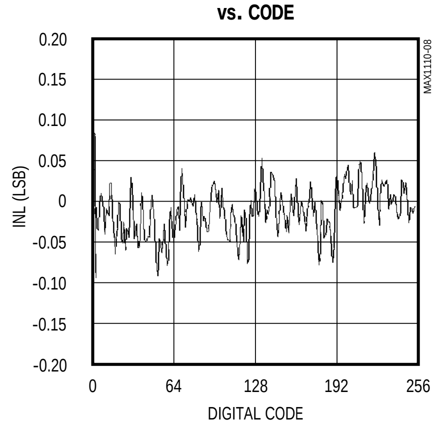
DIFFERENTIAL NONLINEARITY vs. CODE



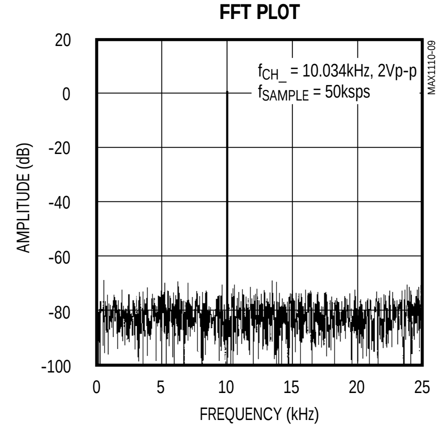
OFFSET ERROR vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. CODE



FFT PLOT



Pin Description

PIN		NAME	FUNCTION
MAX1110	MAX1111		
1–4	1–4	CH0–CH3	Sampling Analog Inputs
5–8	—	CH4–CH7	Sampling Analog Inputs
9	5	COM	Ground Reference for Analog Inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	6	$\overline{SHDN}$	Three-Level Shutdown Input. Normally floats. Pulling $\overline{SHDN}$ low shuts the MAX1110/MAX1111 down to 10µA (max) supply current; otherwise, the devices are fully operational. Pulling $\overline{SHDN}$ high shuts down the internal reference.
11	7	REFIN	Reference Voltage Input for Analog-to-Digital Conversion. Connect to REFOUT to use the internal reference.
12	8	REFOUT	Internal Reference Generator Output. Bypass with a 1µF capacitor to AGND.
13	9	AGND	Analog Ground
14	10	DGND	Digital Ground
15	11	DOUT	Serial-Data Output. Data is clocked out on SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	12	SSTRB	Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1110/MAX1111 begin the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for two clock periods before the MSB is shifted out. High impedance when $\overline{CS}$ is high (external clock mode only).
17	13	DIN	Serial-Data Input. Data is clocked in at SCLK's rising edge. The voltage at DIN may exceed V_{DD} (up to 5.5V).
18	14	$\overline{CS}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance. The voltage at $\overline{CS}$ may exceed V_{DD} (up to 5.5V).
19	15	SCLK	Serial-Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed (duty cycle must be 45% to 55%). The voltage at SCLK may exceed V_{DD} (up to 5.5V).
20	16	V_{DD}	Positive Supply Voltage, +2.7V to +5.5V

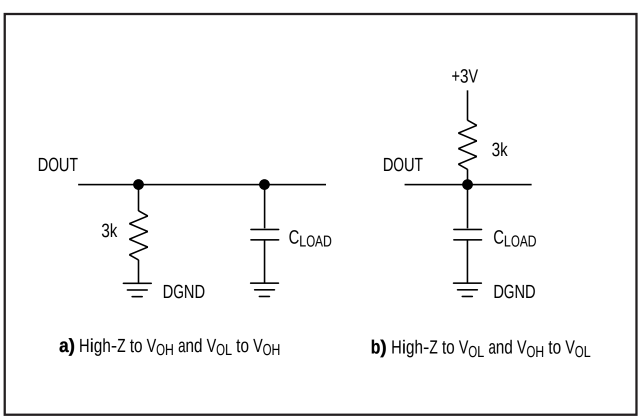


Figure 1. Load Circuits for Enable Time

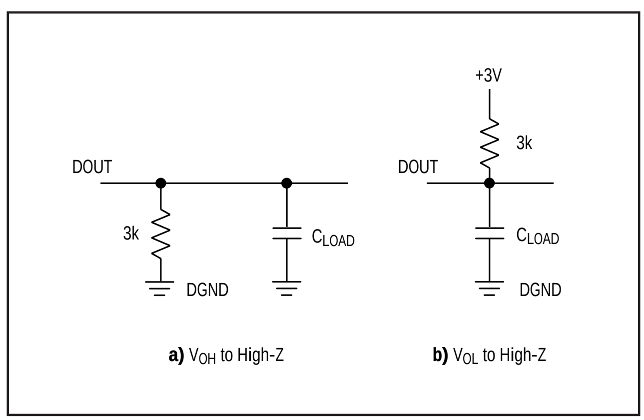


Figure 2. Load Circuits for Disable Time

Detailed Description

The MAX1110/MAX1111 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 shows the Typical Operating Circuit.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in Figure 4, the equivalent input circuit. In single-ended mode, IN+ is internally switched to the selected input channel, CH_, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the MAX1110 channels with Table 1 and the MAX1111 channels with Table 2.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans two SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+. The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 8-bit resolution. This action is equivalent to transferring a charge of 18pF x (V_{IN+} - V_{IN-}) from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the sixth bit of the 8-bit control byte has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control byte has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input; if it is set up for differential inputs, IN- connects to the "-" input, and the difference (IN+ - IN-) is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

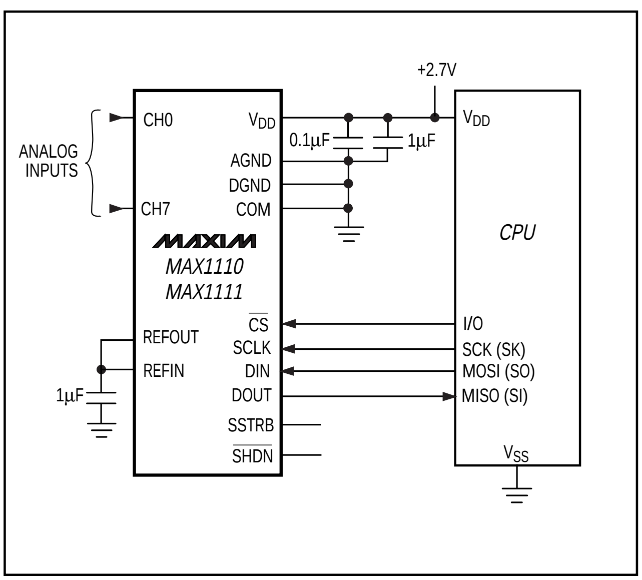


Figure 3. Typical Operating Circuit

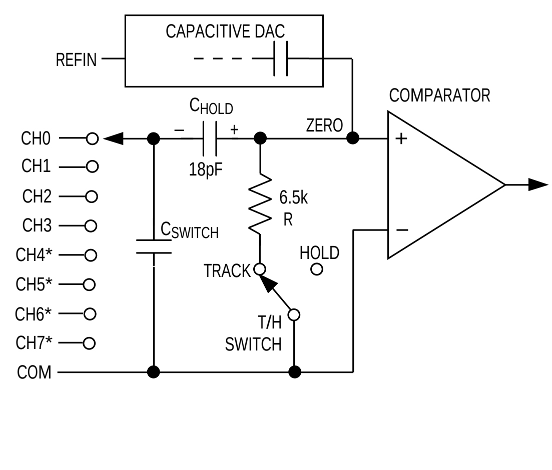


Table 1a. MAX1110 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 1b. MAX1110 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

Table 2a. MAX1111 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	X	+				–
1	0	X		+			–
0	1	X			+		–
1	1	X				+	–

Table 2b. MAX1111 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	X	+	–		
0	1	X			+	–
1	0	X	–	+		
1	1	X			–	+

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 6 \times (R_S + R_{IN}) \times 18pF$$

where R_{IN} = 6.5kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1µs. Note that source impedances below 2.4kΩ do not significantly affect the AC performance of the ADC.

Input Bandwidth

The ADC's input tracking circuitry has a 1.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Inputs

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from (AGND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

The MAX1110/MAX1111 can be configured for differential or single-ended inputs with bits 2 and 3 of the control byte (Table 3). In single-ended mode, the analog inputs are internally referenced to COM with a full-scale input range from COM to V_{REFIN} + COM. For bipolar operation, set COM to V_{REFIN} / 2.

In differential mode, choosing unipolar mode sets the differential input range at 0V to V_{REFIN}. In unipolar mode, the output code is invalid (code zero) when a negative differential input voltage is applied. Bipolar mode sets the differential input range to $\pm V_{REFIN}$ / 2. Note that in this mode, the common-mode input range includes both supply rails. Refer to Table 4 for input voltage ranges.

Quick Look

To quickly evaluate the MAX1110/MAX1111's analog performance, use the circuit of Figure 5. The MAX1110/MAX1111 require a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds

Table 3. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{\text{BIP}}$	SGL/$\overline{\text{DIF}}$	PD1	PD0

BIT	NAME	DESCRIPTION
7 (MSB)	START	The first logic "**1**" bit after $\overline{\text{CS}}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	Select which of the input channels are to be used for the conversion (Tables 1 and 2).
3	UNI/$\overline{\text{BIP}}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. Select differential operation if bipolar mode is used. See Table 4.
2	SGL/$\overline{\text{DIF}}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured. See Tables 1 and 2.
1	PD1	**1** = fully operational, **0** = power-down. Selects fully operational or power-down mode.
0 (LSB)	PD0	**1** = external clock mode, **0** = internal clock mode. Selects external or internal clock mode.

in control bytes of $FF (hex), which trigger single-ended, unipolar conversions on CH7 (MAX1110) or

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 50kHz to 500kHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 7 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with two leading zeros and six trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 1ms, to avoid excessive T/H droop.

Digital Inputs

$\overline{CS}$, SCLK, and DIN can accept input signals up to 5.5V, regardless of the supply voltages. This allows the MAX1110/MAX1111 to accept digital inputs from both 3V and 5V systems.

Digital Output

In unipolar input mode, the output is straight binary (Figure 15). For bipolar inputs, the output is two's-complement (Figure 16). Data is clocked out at SCLK's falling edge in MSB-first format.

Clock Modes

The MAX1110/MAX1111 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the devices. Bit PD0 of the control byte programs the clock mode. Figures 8–11 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for two clock periods after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next eight SCLK falling edges (Figure 7). After the eight data bits are clocked out, subsequent clock pulses clock out zeros from the DOUT pin.

SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 9 shows the SSTRB timing in external clock mode.

The conversion must complete in 1ms, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 50kHz, or if serial-clock interruptions could cause the conversion interval to exceed 1ms.

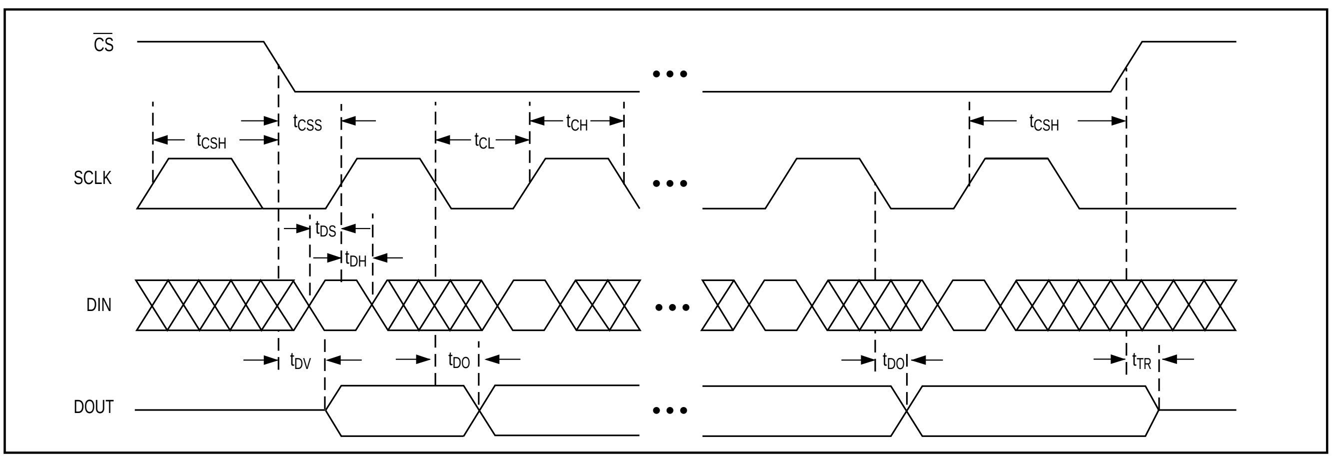
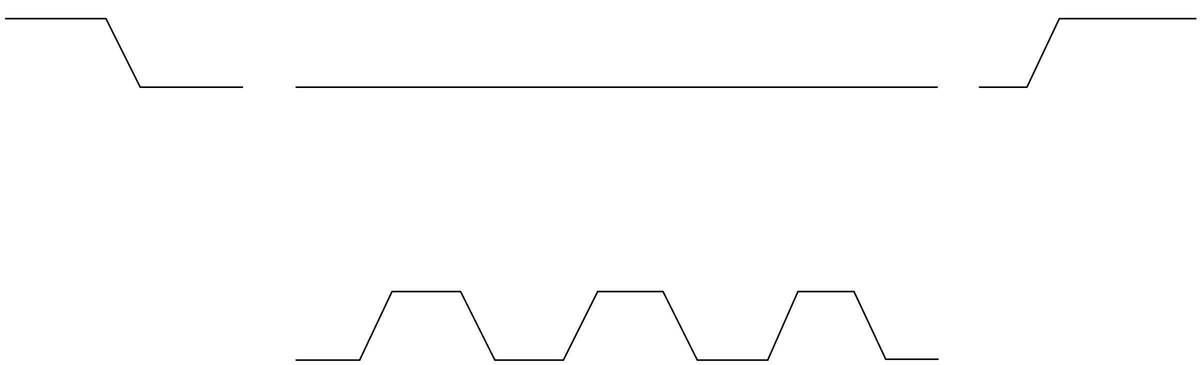


Figure 8. Detailed Serial-Interface Timing



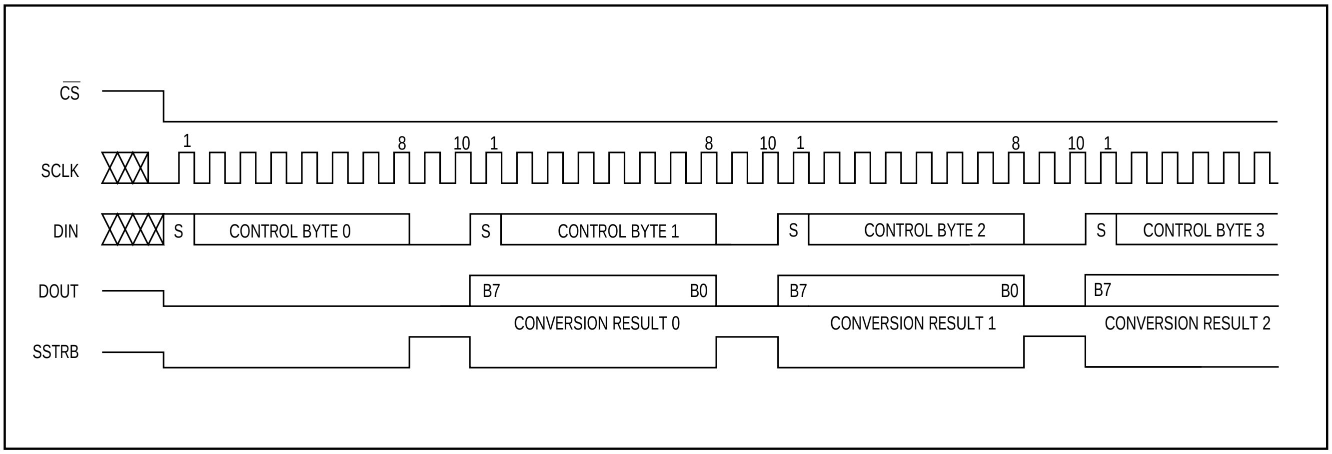


Figure 12a. Continuous Conversions, External Clock Mode, 10 Clocks/Conversion Timing

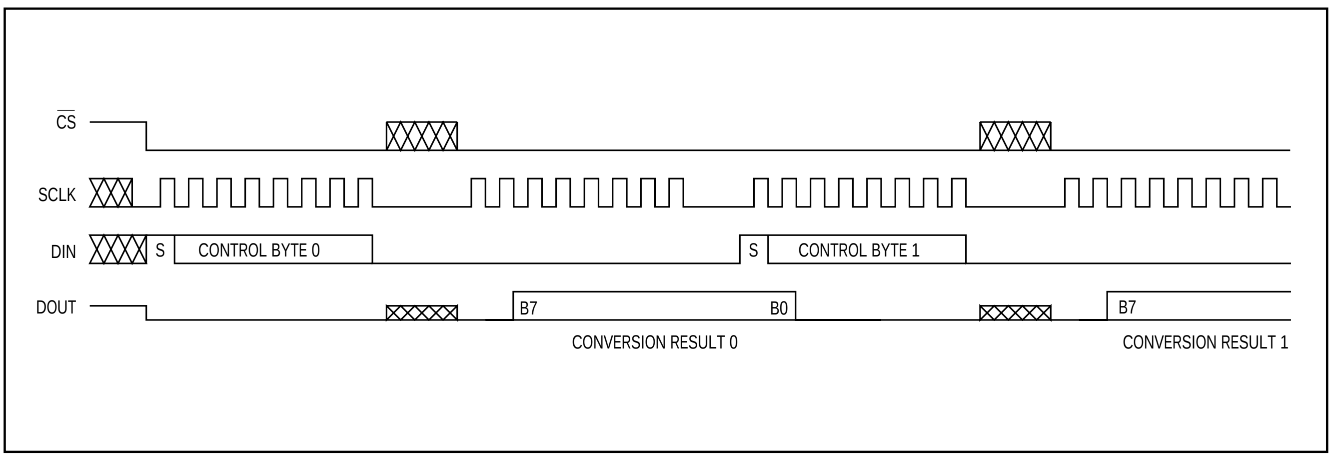


Figure 12b. Continuous Conversions, External Clock Mode, 16 Clocks/Conversion Timing

Data Framing

The falling edge of $\overline{CS}$ does not start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

> The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.
>
> OR
>
> The first high bit clocked into DIN after the MSB of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1110/MAX1111 can run is 10 clocks per conversion. Figure 12a shows the serial-interface timing necessary to perform a conversion every 10 SCLK cycles in external clock mode.

Many microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1110/MAX1111. Figure 12b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

+2.7V, Low-Power, Multichannel, Serial 8-Bit ADCs

Applications Information

Power-On Reset

When power is first applied, and if $\overline{\text{SHDN}}$ is not pulled low, internal power-on reset circuitry activates the MAX1110/MAX1111 in internal clock mode. SSTRB is high on power-up and, if $\overline{\text{CS}}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. No conversions should be performed until the reference voltage has stabilized (see *Electrical Characteristics*).

Power-Down

When operating at speeds below the maximum sampling rate, the MAX1110/MAX1111's automatic power-down mode can save considerable power by placing the converters in a low-current shutdown state between conversions. Figure 13 shows the average supply current as a function of the sampling rate.

Select power-down with PD1 of the DIN control byte with $\overline{\text{SHDN}}$ high or floating (Table 3). Pull $\overline{\text{SHDN}}$ low at any time to shut down the converters completely. $\overline{\text{SHDN}}$ overrides PD1 of the control byte. Figures 14a and 14b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bit PD1 of the control byte. When software power-down is asserted, the ADCs continue to operate in the last specified clock mode until the conversion is complete. The ADCs then power down into a low quiescent-current state. In internal clock mode, the interface remains active, and conversion results may be clocked out after the MAX1110/MAX1111 have entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit, which powers up the MAX1110/MAX1111. If the DIN byte contains PD1 = 1, then the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

Table 5. Hard-Wired Power-Down and Internal Reference State

$\overline{\text{SHDN}}$ STATE	DEVICE MODE	INTERNAL REFERENCE
1	Enabled	Disabled
Floating	Enabled	Enabled
0	Power-Down	Disabled

Hard-Wired Power-Down

Pulling $\overline{\text{SHDN}}$ low places the converters in hard-wired power-down. Unlike software power-down, the conversion is not completed; it stops coincidentally with $\overline{\text{SHDN}}$ being brought low. $\overline{\text{SHDN}}$ also controls the state of the internal reference (Table 5). Letting $\overline{\text{SHDN}}$ float enables the internal 2.048V voltage reference. When returning to normal operation with $\overline{\text{SHDN}}$ floating, there is a t_{RC} delay of approximately 1MΩ x C_{LOAD}, where C_{LOAD} is the capacitive loading on the $\overline{\text{SHDN}}$ pin. Pulling $\overline{\text{SHDN}}$ high disables the internal reference, which saves power when using an external reference.

External Reference

An external reference between 1V and V_{DD} should be connected directly at the REFIN terminal. The DC input impedance at REFIN is extremely high, consisting of leakage current only (typically 10nA). During a conversion, the reference must be able to deliver up to 20µA average load current and have an output impedance of 1kΩ or less at the conversion clock frequency. If the reference has higher output impedance or is noisy, bypass it close to the REFIN pin with a 0.1µF capacitor.

If an external reference is used with the MAX1110/MAX1111, tie $\overline{\text{SHDN}}$ to V_{DD} to disable the internal reference and decrease power consumption.

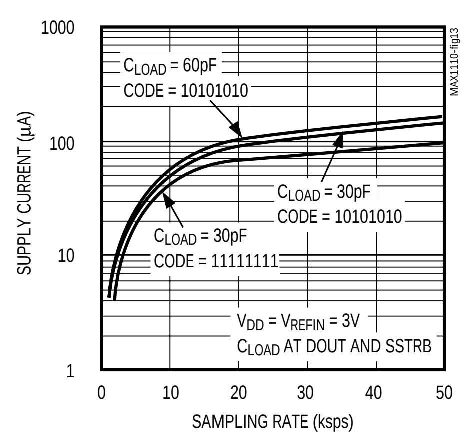


Figure 13. Average Supply Current vs. Sampling Rate

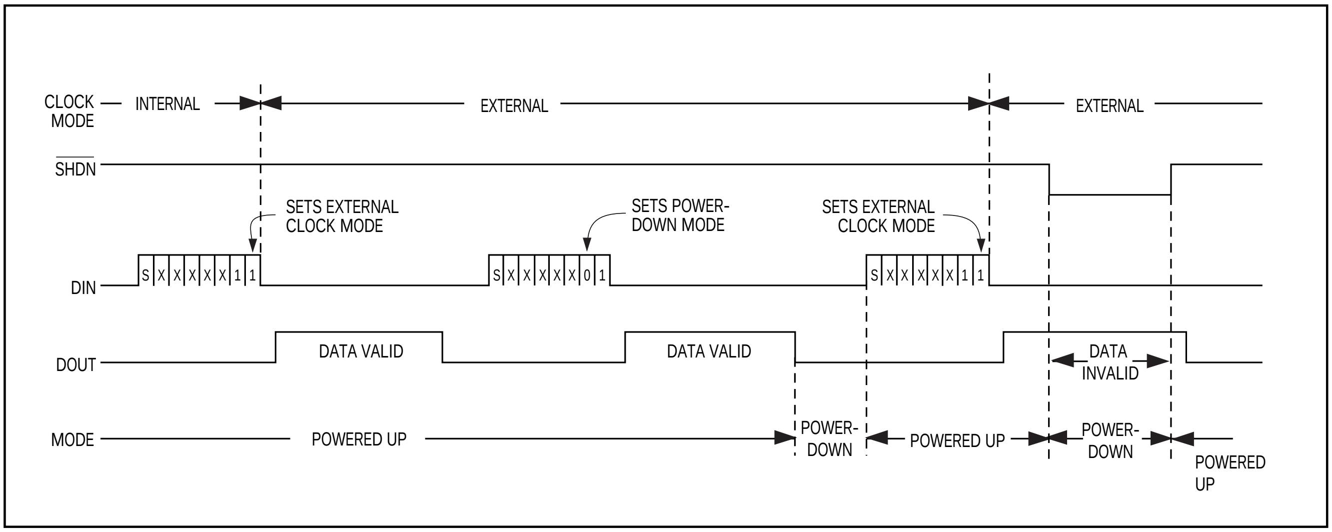


Figure 14a. Power-Down Modes, External Clock Timing Diagram

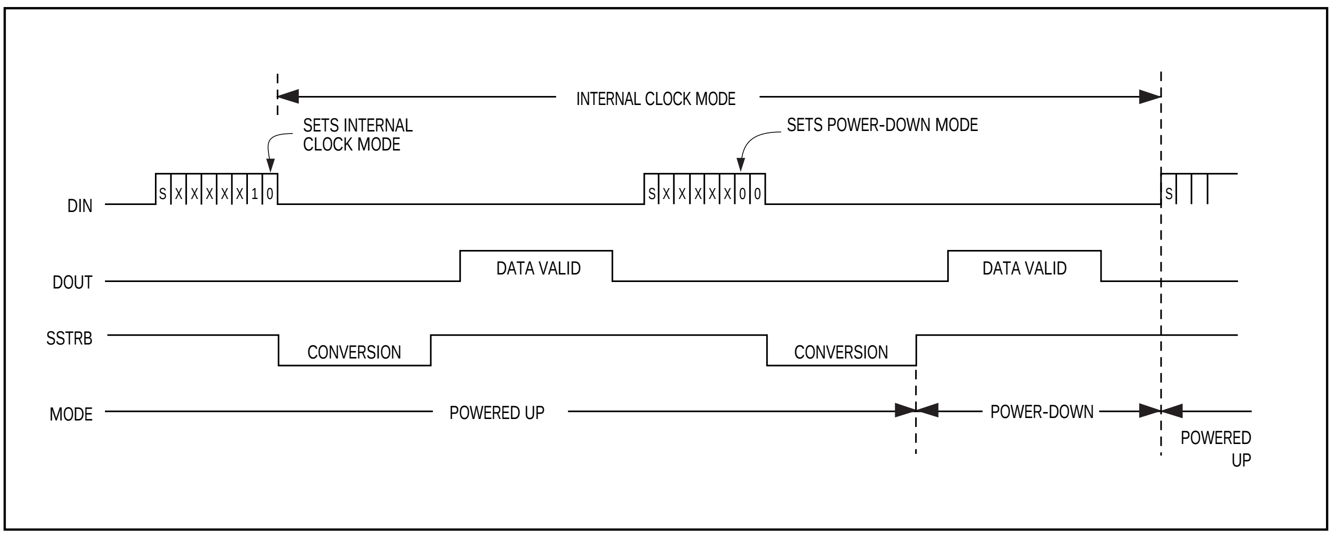


Figure 14b. Power-Down Modes, Internal Clock Timing Diagram

Internal Reference

To use the MAX1110/MAX1111 with the internal reference, connect REFIN to REFOUT. The full-scale range of the MAX1110/MAX1111 with the internal reference is typically 2.048V with unipolar inputs, and ±1.024V with bipolar inputs. The internal reference should be bypassed to AGND with a 1µF capacitor placed as close to the REFIN pin as possible.

Transfer Function

Table 4 shows the full-scale voltage ranges for unipolar and bipolar modes. Figure 15 depicts the nominal, unipolar I/O transfer function, and Figure 16 shows the bipolar I/O transfer function when using a 2.048V reference. Code transitions occur at integer LSB values. Output coding is binary, with 1LSB = 8mV (2.048V/256) for unipolar operation and 1LSB = 8mV [(2.048V/2 - -2.048V/2)/256] for bipolar operation.

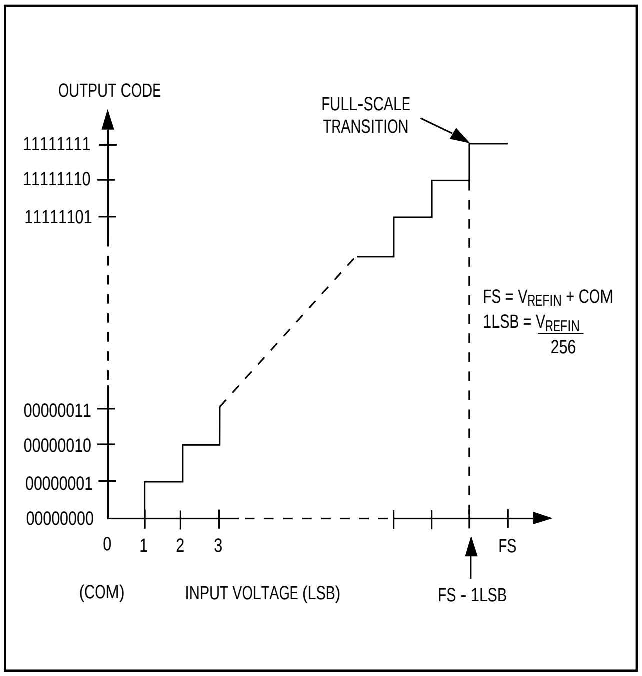


Figure 15. Unipolar Transfer Function

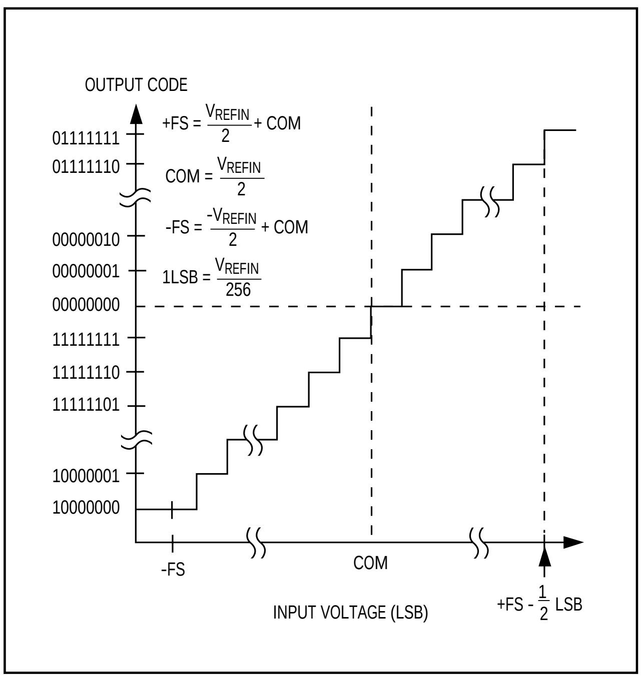


Figure 16. Bipolar Transfer Function

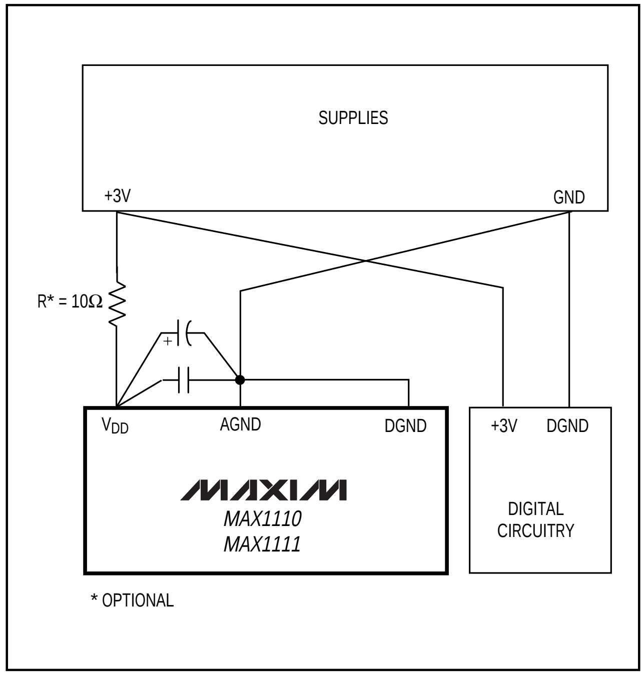


Figure 17. Power-Supply Grounding Connections

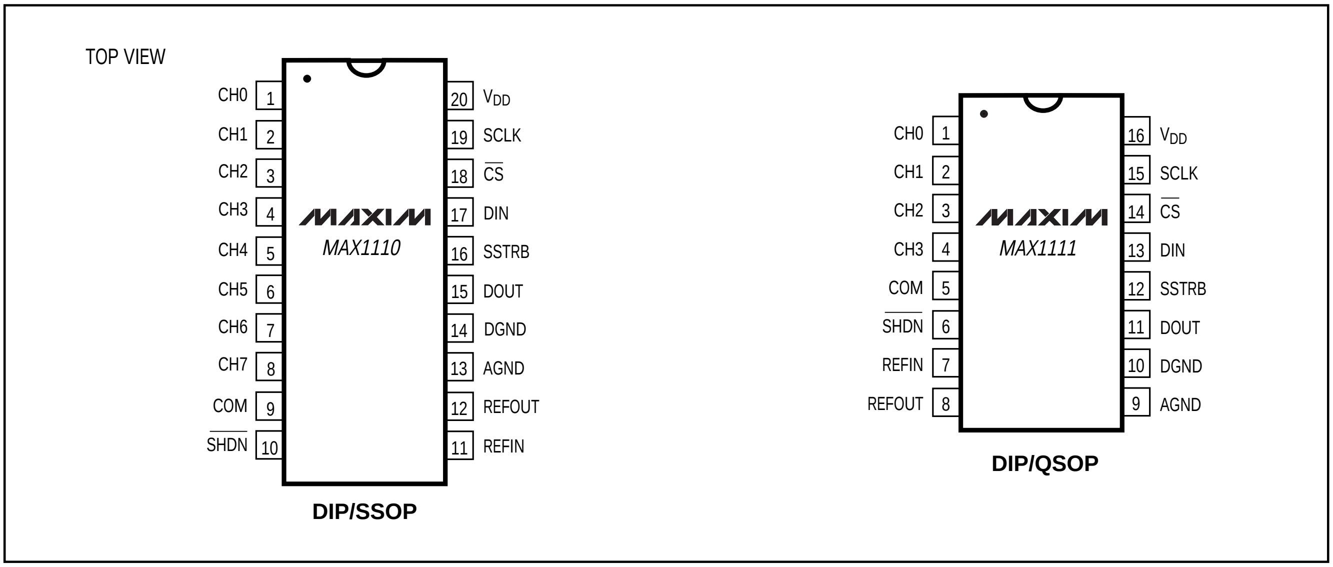
Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground (star ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to the V_{DD} pin of the MAX1110/MAX1111. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected to form a lowpass filter.

Pin Configurations



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX1110EPP	-40°C to +85°C	20 Plastic DIP
MAX1110EAP	-40°C to +85°C	20 SSOP
MAX1110MJP	-55°C to +125°C	20 CERDIP**
MAX1111CPE	0°C to +70°C	16 Plastic DIP
MAX1111CEE	0°C to +70°C	16 QSOP
MAX1111EPE	-40°C to +85°C	16 Plastic DIP
MAX1111EEE	-40°C to +85°C	16 QSOP
MAX1111MJE	-55°C to +125°C	16 CERDIP**

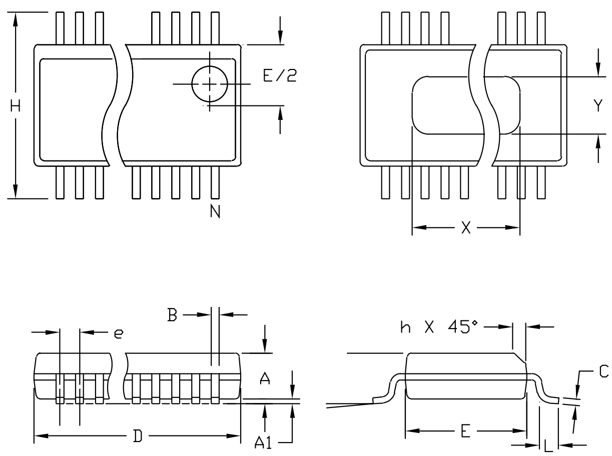
***Contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 1996

SUBSTRATE CONNECTED TO DGND

Package Information



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
X	.107	.123	2.72	3.12		
D	.386	.393	9.80	9.98	28	AD
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV B | 1/1