# Precision JFET, High Speed, Dual Operational Amplifier

# OP249

## FEATURES

**Fast slew rate: 22 V/µs typical**
**Settling time (0.01%): 1.2 µs maximum**
**Offset voltage: 200 µV typical**
**High open-loop gain: 1000 V/mV minimum**
**Low total harmonic distortion: 0.002% typical**

## APPLICATIONS

**Output amplifier for fast DACs**
**Signal processing**
**Instrumentation amplifiers**
**Fast sample-and-holds**
**Active filters**
**Low distortion audio amplifiers**
**Input buffer for ADCs**
**Servo controllers**

## PIN CONFIGURATIONS

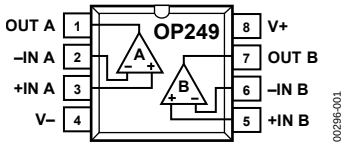


*Figure 1. 8-Lead CERDIP (Q-8) and 8-Lead PDIP (N-8)*

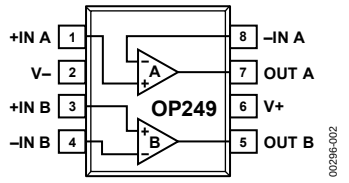


*Figure 2. 8-Lead SOIC (R-8)*

## GENERAL DESCRIPTION

The OP249 is a high speed, precision dual JFET op amp, similar to the popular single op amp. The OP249 outperforms available dual amplifiers by providing superior speed with excellent dc performance. Ultrahigh open-loop gain (1 kV/mV minimum), low offset voltage, and superb gain linearity makes the OP249 the industry's first true precision, dual high speed amplifier.

With a slew rate of 22 V/µs typical and a fast settling time of less than 1.2 µs maximum to 0.01%, the OP249 is an ideal choice for high speed bipolar DAC and ADC applications. The excellent dc performance of the OP249 allows the full accuracy of high resolution CMOS DACs to be realized.

Symmetrical slew rate, even when driving large load, such as, 600 Ω or 200 pF of capacitance and ultralow distortion, make the OP249 ideal for professional audio applications, active filters, high speed integrators, servo systems, and buffer amplifiers.

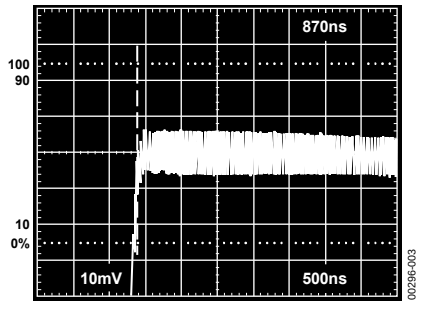


*Figure 3. Fast Settling (0.01%)*

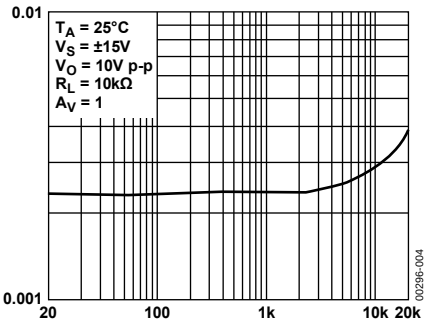


*Figure 4. Low Distortion, $A_V$ = 1, $R_L$ = 10 kΩ*

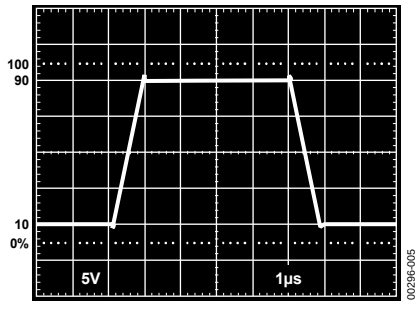


*Figure 5. Excellent Output Drive, $R_L$ = 600 Ω*

**Rev. G**
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## REVISION HISTORY

**4/10—Rev. F to Rev. G**

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**5/07—Rev. E to Rev. F**

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**9/01—Rev. D to Rev. E**

Edits to Features and Pin Connections ..... 1
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# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_S$ = ±15 V, $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| | | | OP249A | | | OP249F | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0 V | | 0.2 | 0.75 | | 0.2 | 0.9 | mV |
| Offset Stability | | | | 1.5 | | | 1.5 | | µV/month |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0 V, $T_A$ = 25°C | | 30 | 75 | | 30 | 75 | pA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 0 V, $T_A$ = 25°C | | 6 | 25 | | 6 | 25 | pA |
| Input Voltage Range[1] | IVR | | | 12.5 | | | 12.5 | | V |
| | | | ±11 | | | ±11 | | | V |
| | | | | −12.5 | | | −12.5 | | V |
| Common-Mode Rejection | CMR | $V_{CM}$ = ±11 V | 80 | 90 | | 80 | 90 | | dB |
| Power-Supply Rejection Ratio | PSRR | $V_S$ = ± 4.5 V to ±18 V | | 12 | 31.6 | | 12 | 50 | µV/V |
| Large Signal Voltage Gain | $A_{VO}$ | $V_O$ = ±10 V, $R_L$ = 2 kΩ | 1000 | 1400 | | 500 | 1200 | | V/mV |
| Output Voltage Swing | $V_O$ | $R_L$ = 2 kΩ | | 12.5 | | | 12.5 | | V |
| | | | ±12.0 | | | ±12.0 | | | V |
| | | | | −12.5 | | | −12.5 | | V |
| Short-Circuit Current Limit | $I_{SC}$ | Output shorted to ground | | 36 | | | 36 | | mA |
| | | | ±20 | | ±50 | ±20 | | ±50 | mA |
| | | | | −33 | | | −33 | | mA |
| Supply Current | $I_{SY}$ | No load, $V_O$ = 0 V | | 5.6 | 7.0 | | 5.6 | 7.0 | mA |
| Slew Rate | SR | $R_L$ = 2 kΩ, $C_L$ = 50 pF | 18 | 22 | | 18 | 22 | | V/µs |
| Gain Bandwidth Product[2] | GBW | | 3.5 | 4.7 | | 3.5 | 4.7 | | MHz |
| Settling Time | $t_S$ | 10 V step 0.01%[3] | | 0.9 | 1.2 | | 0.9 | 1.2 | µs |
| Phase Margin | $\Theta_M$ | 0 dB gain | | 55 | | | 55 | | Degrees |
| Differential Input Impedance | $Z_{IN}$ | | | $10^{12}$\|\|6 | | | $10^{12}$\|\|6 | | Ω\|\|pF |
| Open-Loop Output Resistance | $R_O$ | | | 35 | | | 35 | | Ω |
| Voltage Noise | $e_n$ p-p | 0.1 Hz to 10 Hz | | 2 | | | 2 | | µV p-p |
| Voltage Noise Density | $e_n$ | $f_O$ = 10 Hz | | 75 | | | 75 | | nV/√Hz |
| | | $f_O$ = 100 Hz | | 26 | | | 26 | | nV/√Hz |
| | | $f_O$ = 1 kHz | | 17 | | | 17 | | nV/√Hz |
| | | $f_O$ = 10 kHz | | 16 | | | 16 | | nV/√Hz |
| Current Noise Density | $i_n$ | $f_O$ = 1 kHz | | 0.003 | | | 0.003 | | pA/√Hz |
| Voltage Supply Range | $V_S$ | | ±4.5 | ±15 | ±18 | ±4.5 | ±15 | ±18 | V |

[1] Guaranteed by CMR test.
[2] Guaranteed by design.
[3] Settling time is sample tested.

$V_S$ = ±15 V, $T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| | | | OP249G | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0 V | | 0.4 | 2.0 | mV |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0 V, $T_A$ = 25°C | | 40 | 75 | pA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 0 V $T_A$ = 25°C | | 10 | 25 | pA |
| Input Voltage Range[1] | IVR | | | 12.5 | | V |
| | | | ±11 | | | V |
| | | | | −12.0 | | V |
| Common-Mode Rejection | CMR | $V_{CM}$ = ±11 V | 76 | 90 | | dB |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±4.5 V to ±18 V | | 12 | 50 | µV/V |
| Large Signal Voltage Gain | $A_{VO}$ | $V_O$ = ±10 V; $R_L$ = 2 kΩ | 500 | 1100 | | V/mV |
| Output Voltage Swing | $V_O$ | $R_L$ = 2 kΩ | | 12.5 | | V |
| | | | ±12.0 | | | V |
| | | | | −12.5 | | V |
| Short-Circuit Current Limit | $I_{SC}$ | Output shorted to ground | | 36 | | mA |
| | | | ±20 | | ±50 | mA |
| | | | | −33 | | mA |
| Supply Current | $I_{SY}$ | No load; $V_O$ = 0 V | | 5.6 | 7.0 | mA |
| Slew Rate | SR | $R_L$ = 2 kΩ, $C_L$ = 50 pF | 18 | 22 | | V/µs |
| Gain Bandwidth Product[2] | GBW | | | 4.7 | | MHz |
| Settling Time | $t_S$ | 10 V step 0.01% | | 0.9 | 1.2 | µs |
| Phase Margin | $\Theta_M$ | 0 dB gain | | 55 | | Degree |
| Differential Input Impedance | $Z_{IN}$ | | | $10^{12}$\|\|6 | | Ω\|\|pF |
| Open-Loop Output Resistance | $R_O$ | | | 35 | | Ω |
| Voltage Noise | $e_n$ p-p | 0.1 Hz to 10 Hz | | 2 | | µV p-p |
| Voltage Noise Density | $e_n$ | $f_O$ = 10 Hz | | 75 | | nV/√Hz |
| | | $f_O$ = 100 Hz | | 26 | | nV/√Hz |
| | | $f_O$ = 1 kHz | | 17 | | nV/√Hz |
| | | $f_O$ = 10 kHz | | 16 | | nV/√Hz |
| Current Noise Density | $i_n$ | $f_O$ = 1 kHz | | 0.003 | | pA/√Hz |
| Voltage Supply Range | $V_S$ | | ±4.5 | ±15 | ±18 | V |

[1] Guaranteed by CMR test.
[2] Guaranteed by design.

# ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter[1] | Rating |
|---|---|
| Supply Voltage | ±18 V |
| Input Voltage[2] | ±18 V |
| Differential Input Voltage[2] | 36 V |
| Output Short-Circuit Duration | Indefinite |
| Storage Temperature Range | −65°C to +175°C |
| Operating Temperature Range | |
| OP249A (Q) | −55°C to +125°C |
| OP249F (Q) | −40°C to +85°C |
| OP249G (N, R) | −40°C to +85°C |
| Junction Temperature Range | |
| OP249A (Q), OP249F (Q) | −65°C to +175°C |
| OP249G (N, R) | −65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |

[1] Absolute maximum ratings apply to packaged parts, unless otherwise noted.
[2] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 6. Thermal Resistance**

| Package Type | $\theta_{JA}$[1] | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead CERDIP (Q) | 134 | 12 | °C/W |
| 8-Lead PDIP (N) | 96 | 37 | °C/W |
| 8-Lead SOIC (R) | 150 | 41 | °C/W |

[1] $\theta_{JA}$ is specified for worst-case mounting conditions, that is, $\theta_{JA}$ is specified for device in socket for CERDIP and PDIP packages; $\theta_{JA}$ is specified for device soldered to printed circuit board for SOIC package.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

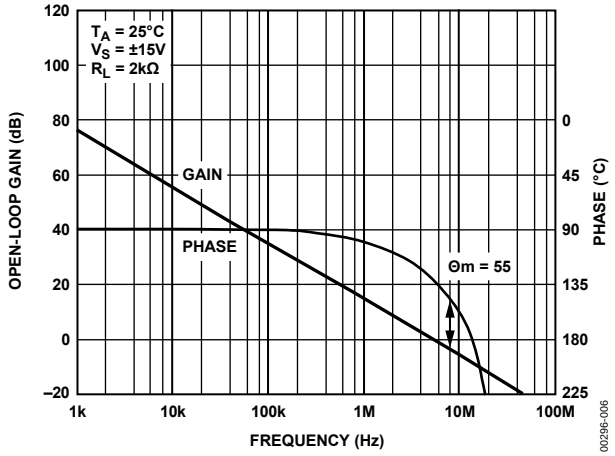


*Figure 6. Open-Loop Gain, Phase vs. Frequency*

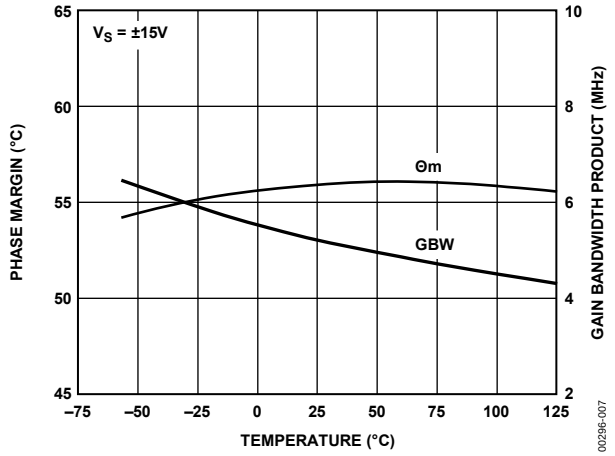


*Figure 7. Phase Margin, Gain Bandwidth Product vs. Temperature*

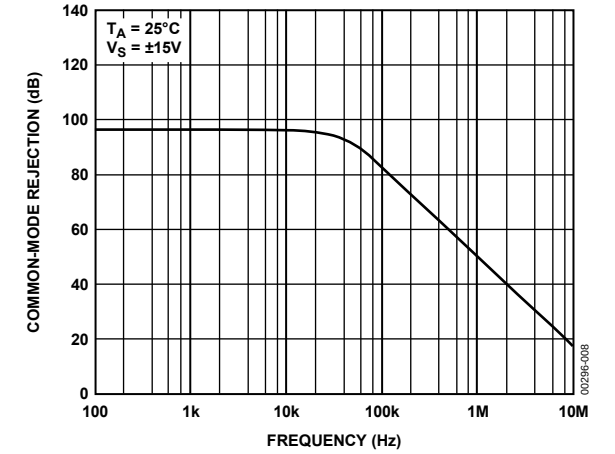


*Figure 8. Common-Mode Rejection vs. Frequency*

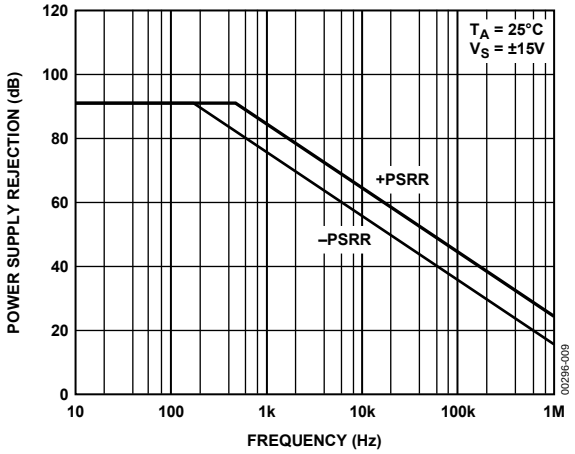


*Figure 9. Power Supply Rejection vs. Frequency*

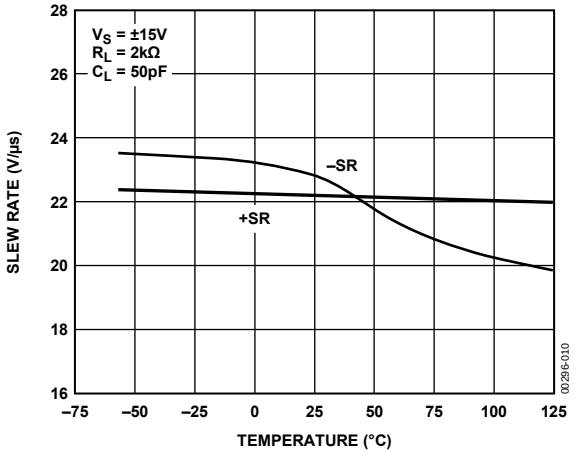


*Figure 10. Slew Rate vs. Temperature*

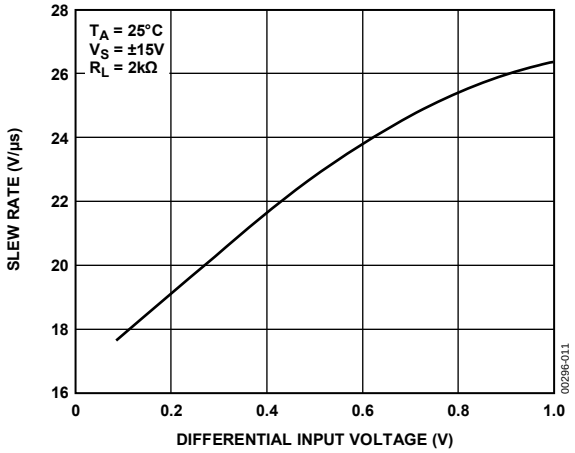


*Figure 11. Slew Rate vs. Differential Input Voltage*

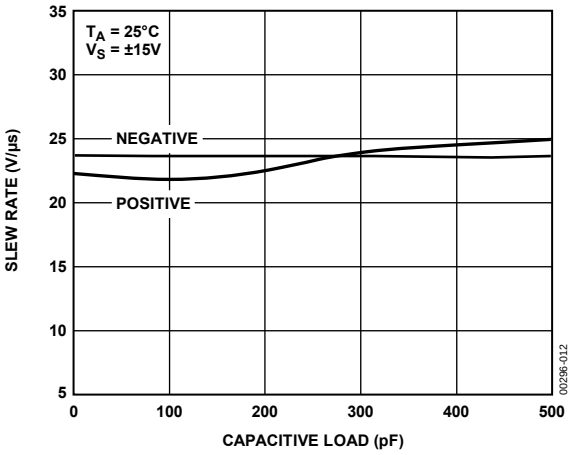


*Figure 12. Slew Rate vs. Capacitive Load*

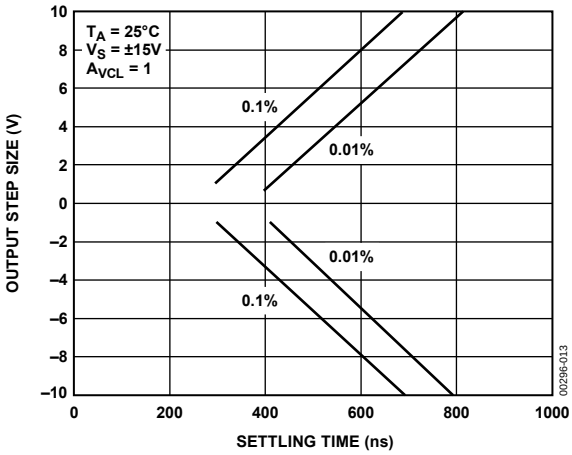


*Figure 13. Step Size vs. Settling Time*

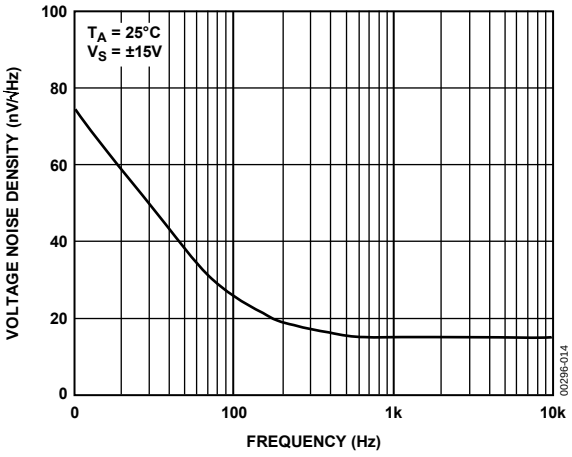


*Figure 14. Voltage Noise Density vs. Frequency*

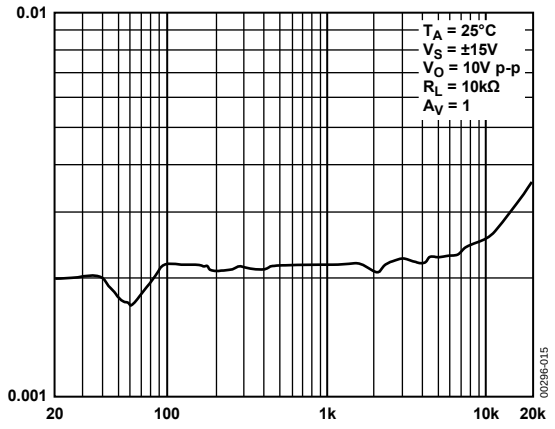


*Figure 15. Distortion vs. Frequency*

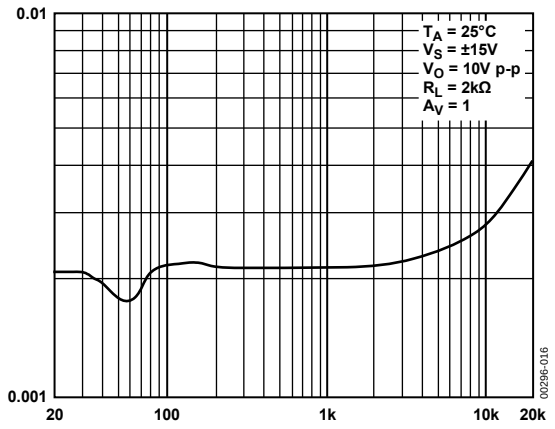


*Figure 16. Distortion vs. Frequency*

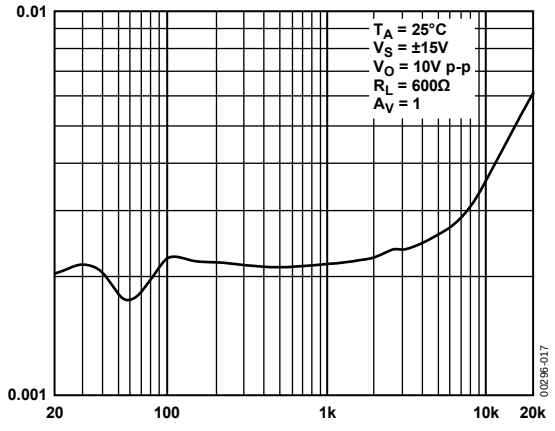


*Figure 17. Distortion vs. Frequency*

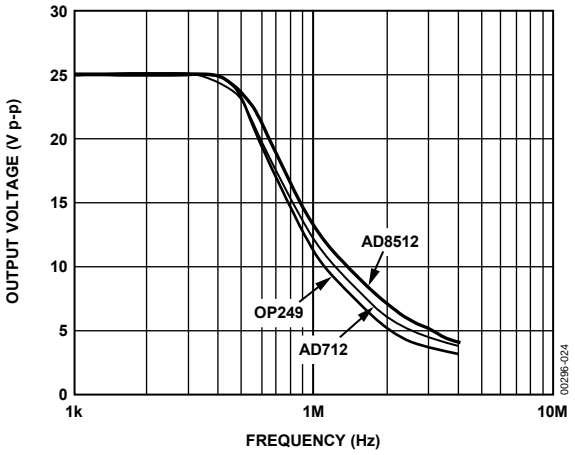


Figure 24. Output Voltage vs. Frequency

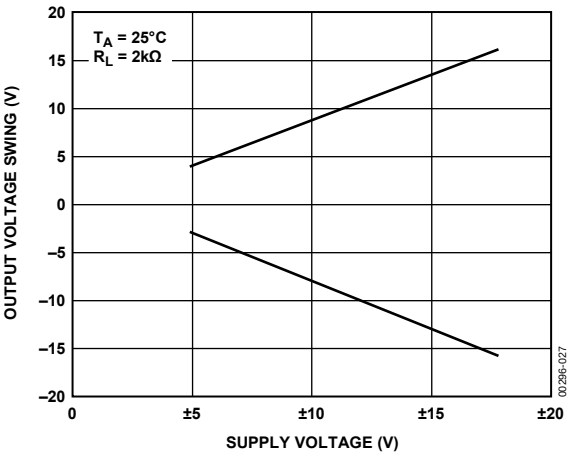


Figure 27. Output Voltage Swing vs. Supply Voltage

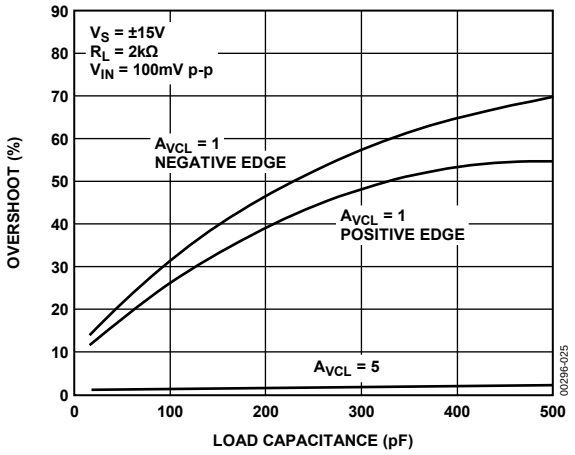


Figure 25. Small Overshoot vs. Load Capacitance

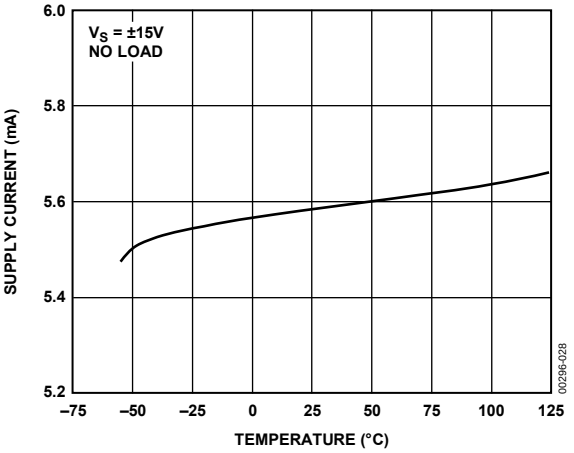


Figure 28. Supply Current vs. Temperature

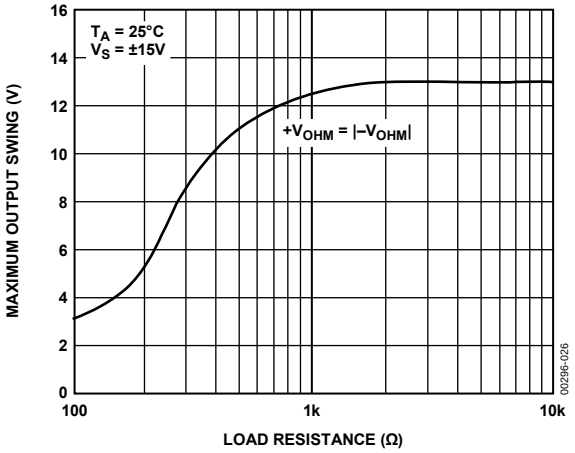


Figure 26. Maximum Output Voltage Swing vs. Load Resistance

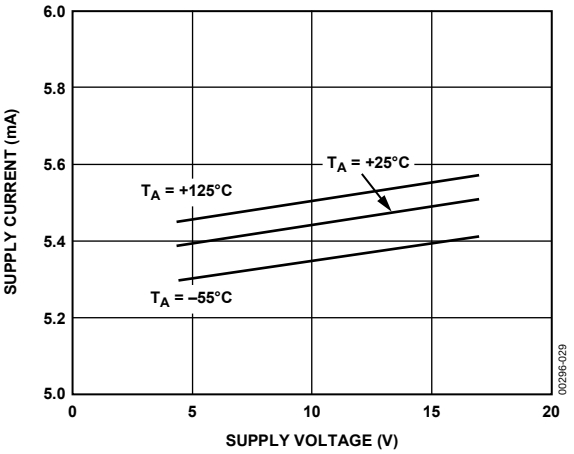


Figure 29. Supply Current vs. Supply Voltage

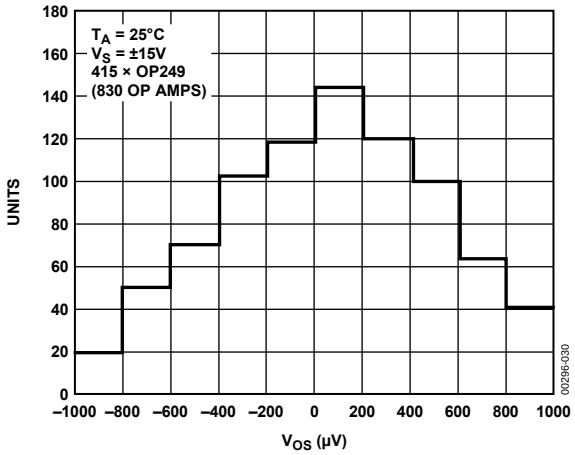


Figure 30. $V_{OS}$ Distribution (N-8)

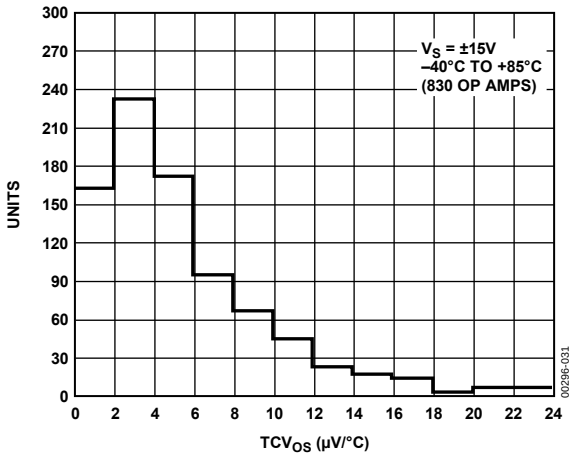


Figure 31. $TCV_{OS}$ Distribution (N-8)

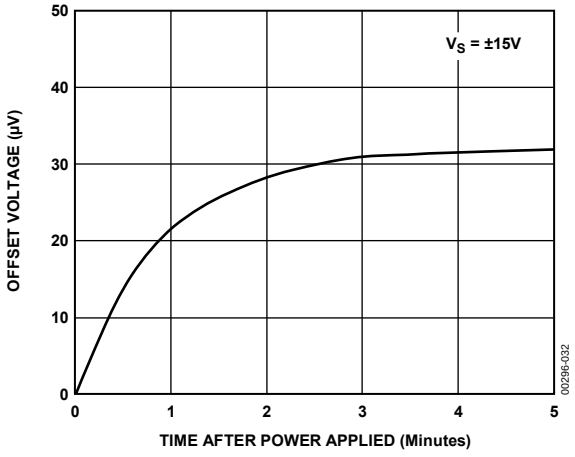


Figure 32. Offset Voltage Warm-Up Drift

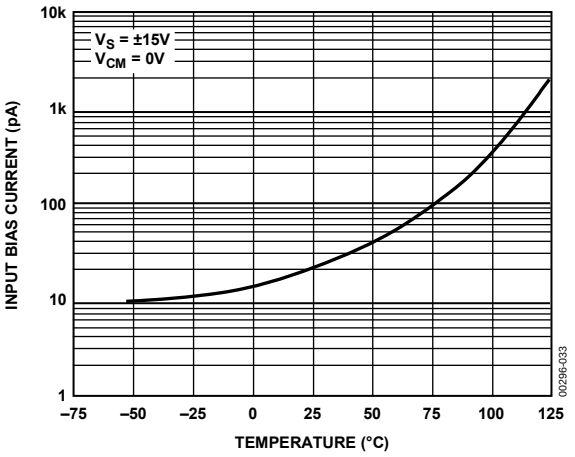


Figure 33. Input Bias Current vs. Temperature

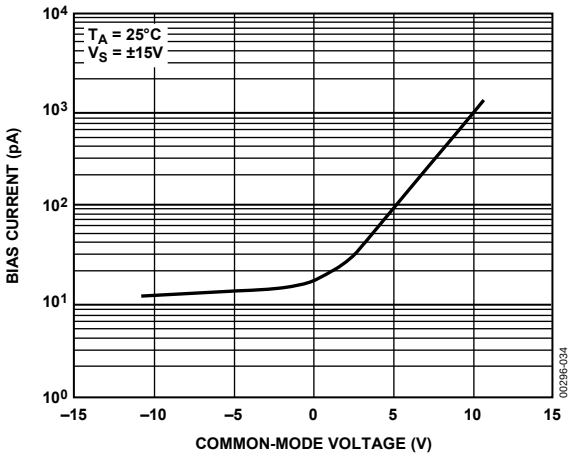


Figure 34. Bias Current vs. Common-Mode Voltage

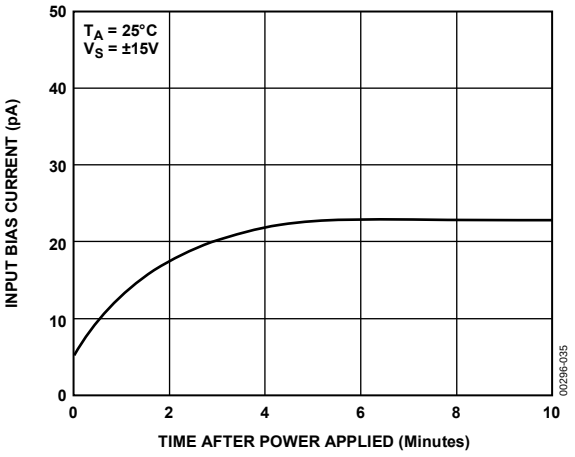


Figure 35. Bias Current Warm-Up Drift

# APPLICATIONS INFORMATION

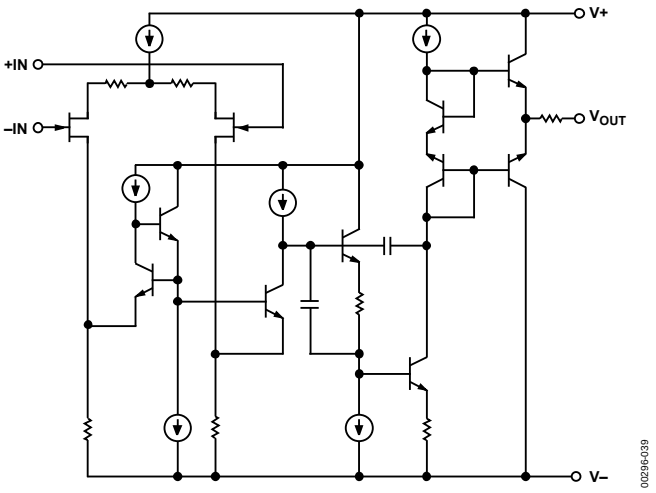


*Figure 39. Simplified Schematic (1/2 OP249)*

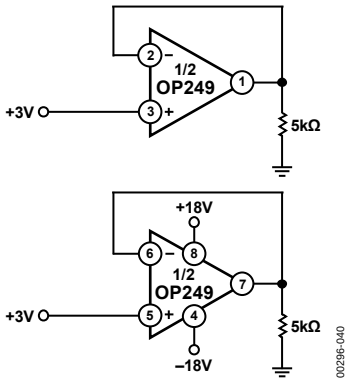


*Figure 40. Burn-In Circuit*

The OP249 represents a reliable JFET amplifier design, featuring an excellent combination of dc precision and high speed. A rugged output stage provides the ability to drive a 600 Ω load and still maintain a clean ac response. The OP249 features a large signal response that is more linear and symmetric than previously available JFET input amplifiers. Figure 41 compares the large signal response of the OP249 to other industry-standard dual JFET amplifiers.

Typically, the slewing performance of the JFET amplifier is specified as a number of V/µs. There is no discussion on the quality, that is, linearity and symmetry of the slewing response.

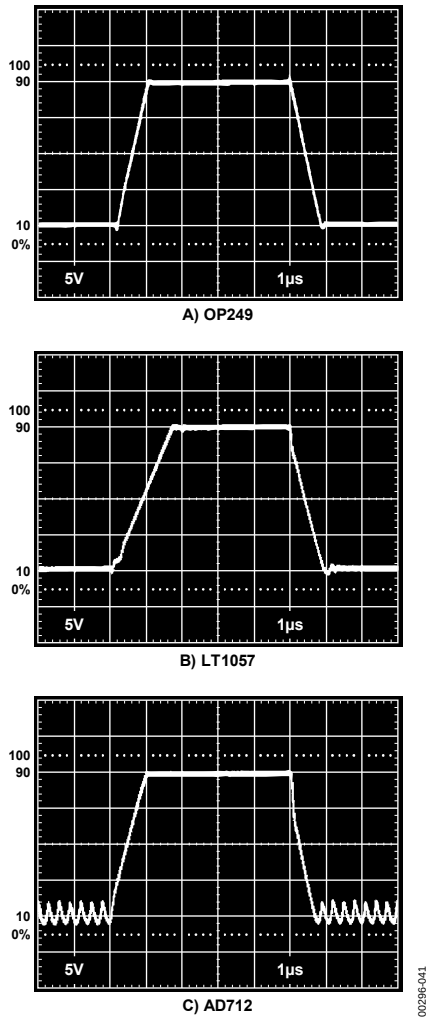


*Figure 41. Large-Signal Transient Response, $A_V$ = 1, $V_{IN}$ = 20 V p-p, $Z_L$ = 2 kΩ//200 pF, $V_S$ = ±15 V*

The OP249 was carefully designed to provide symmetrically

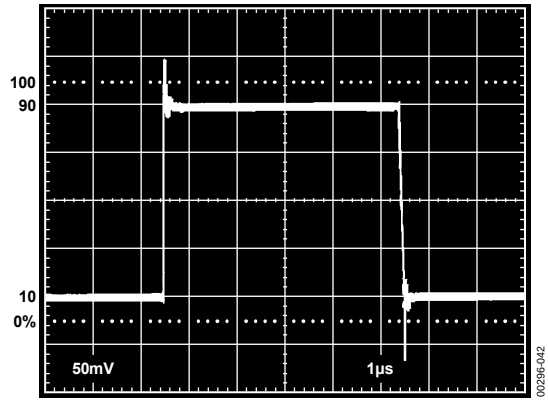


*Figure 42. Small-Signal Transient Response, $A_V$ = 1, $Z_L$ = 2 kΩ||100 pF, No Compensation, $V_S$ = ±15 V*

As with most JFET input amplifiers, the output of the OP249 can undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion does not damage the amplifier, nor does it cause an internal latch-up condition.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier. A 0.1 µF and a 10 µF capacitor should be placed between each supply pin and ground.

## OPEN-LOOP GAIN LINEARITY

The OP249 has both an extremely high open-loop gain of 1 kV/mV minimum and constant gain linearity, which enhances its dc precision and provides superb accuracy in high closed-loop gain applications. Figure 43 illustrates the typical open-loop gain linearity—high gain accuracy is assured, even when driving a 600 Ω load.

## OFFSET VOLTAGE ADJUSTMENT

The inherent low offset voltage of the OP249 makes offset adjustments unnecessary in most applications. However, where a lower offset error is required, balancing can be performed with simple external circuitry, as shown in Figure 44 and Figure 45.

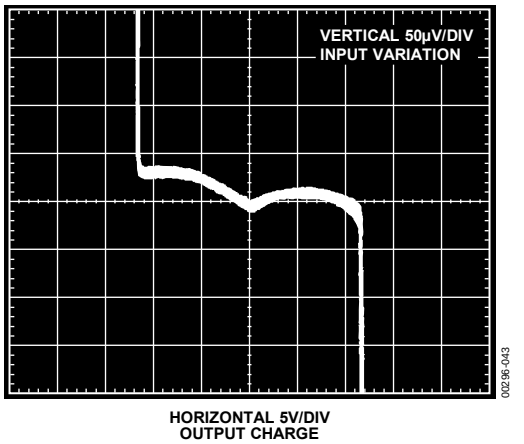


*Figure 43. Open-Loop Gain Linearity; Variation in Open-Loop Gain Results in Errors in High Closed-Loop Gain Circuits; $R_L$ = 600 Ω, $V_S$ = ±15 V*

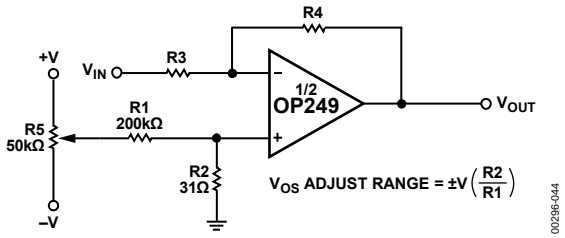


*Figure 44. Offset Adjustment for Inverting Amplifier Configuration*

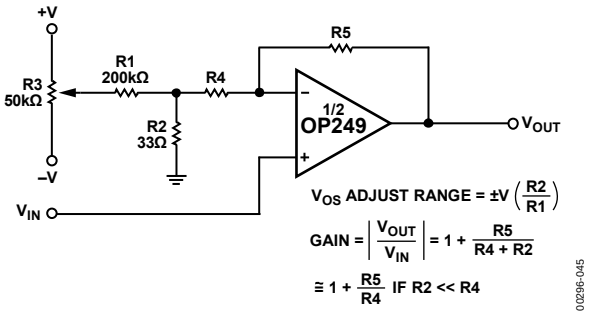


*Figure 45. Offset Adjustment for Noninverting Amplifier Configuration*

In Figure 44, the offset adjustment is made by supplying a small voltage at the noninverting input of the amplifier. Resistors R1 and R2 attenuate the potentiometer voltage, providing a ±2.5 mV (with $V_S$ = ±15 V) adjustment range, referred to the input. Figure 45 shows the offset adjustment for the noninverting amplifier configuration, also providing a ±2.5 mV adjustment range. As shown in the equations in Figure 45, if R4 is not much greater than R2, a resulting closed-loop gain error must be accounted for.

## SETTLING TIME

The settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. The error bands on the output are 5 mV and 0.5 mV, respectively, for 0.1% and 0.01% accuracy.

Figure 46 shows the settling time of the OP249, which is typically 870 ns. Moreover, problems in settling response, such as thermal tails and long-term ringing, are nonexistent.

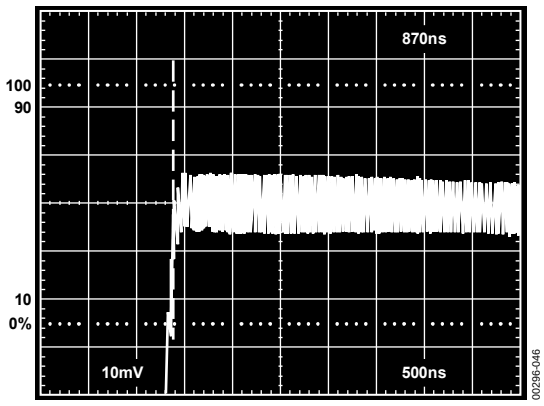


*Figure 46. Settling Characteristics of the OP249 to 0.01%*

## DAC OUTPUT AMPLIFIER

Unity-gain stability, a low offset voltage of 300 μV typical, and a fast settling time of 870 ns to 0.01%, makes the OP249 an ideal amplifier for fast DACs.

For CMOS DAC applications, the low offset voltage of the OP249 results in excellent linearity performance. CMOS DACs, such as the PM7545, typically have a code-dependent output resistance variation between 11 kΩ and 33 kΩ. The change in output resistance, in conjunction with the 11 kΩ feedback resistor, results in a noise gain change, which causes variations in the offset Shape

Because the DAC output capacitance appears at the inputs of the op amp, it is essential that the amplifier be adequately compensated. Compensation increases the phase margin and ensures an optimal overall settling response. The required lead compensation is achieved with Capacitor C in Figure 48.

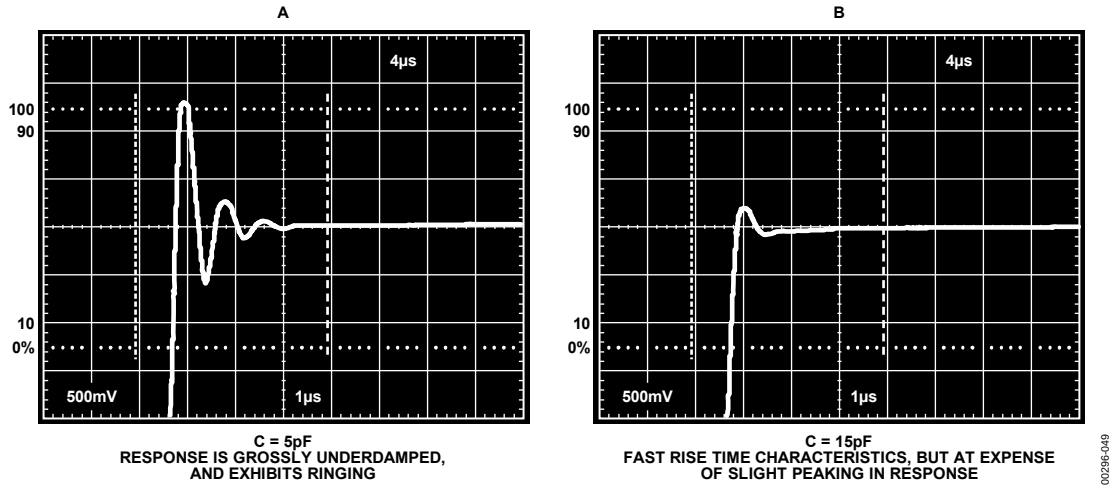


*Figure 49. Effect of Altering Compensation from Circuit in Figure 47—PM7545 CMOS DAC with 1/2 OP249, Unipolar Operation; Critically Damped Response Is Obtained with C ≈ 33 pF*

Figure 49 illustrates the effect of altering the compensation on the output response of the circuit in Figure 47. Compensation is required to address the combined effect of the output capacitance of the DAC, the input capacitance of the op amp, and any stray capacitance. Slight adjustments to the compensation capacitor may be required to optimize settling response for any given application.

The settling time of the combination of the current output DAC and the op amp can be approximated by

$$t_S\ TOTAL = \sqrt{(t_S\ DAC)^2 + (t_S\ AMP)^2}$$

The actual overall settling time is affected by the noise gain of the amplifier, the applied compensation, and the equivalent input capacitance at the input of the amplifier.

## DISCUSSION ON DRIVING ADCs

Settling characteristics of op amps also include the ability of the amplifier to recover, that is, settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR-type ADC. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output settles before the converter makes a comparison decision, which prevents linearity errors or missing codes.

Figure 50 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1 mA.

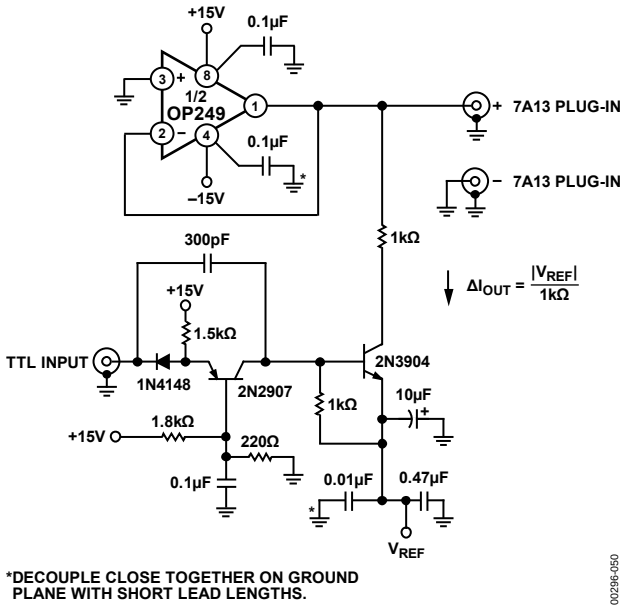


*Figure 50. Transient Output Impedance Test Fixture*

As seen in Figure 51, the OP249 has an extremely fast recovery of 247 ns (to 0.01%) for a 1 mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

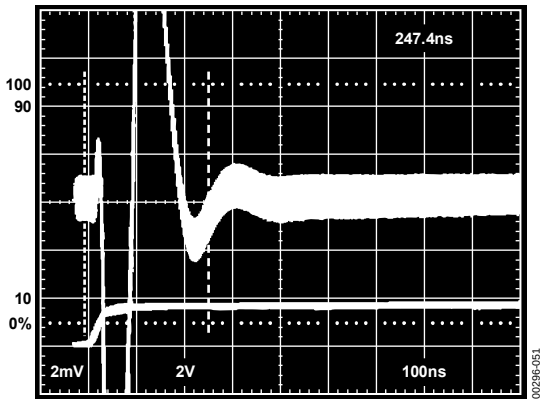


*Figure 51. Transient Recovery Time of the OP249 from a 1 mA Load Transient to 0.01%*

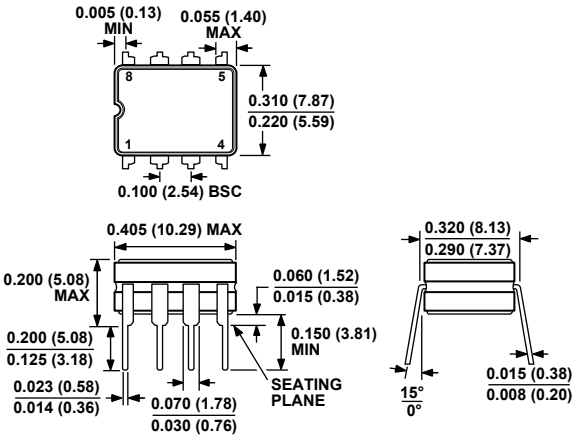


*Figure 54. 8-Lead Ceramic Dual In-Line Package [CERDIP]*
*(Q-8)*
*Dimensions shown in inches and (millimeters)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| OP249AZ | −55°C to +125°C | 8-Lead CERDIP | Q-8 |
| OP249FZ | −40°C to +85°C | 8-Lead CERDIP | Q-8 |
| OP249GP | −40°C to +85°C | 8-Lead PDIP | N-8 |
| OP249GPZ | −40°C to +85°C | 8-Lead PDIP | N-8 |
| OP249GS | −40°C to +85°C | 8-Lead SOIC_N | R-8 |
| OP249GS-REEL | −40°C to +85°C | 8-Lead SOIC_N | R-8 |
| OP249GS-REEL7 | −40°C to +85°C | 8-Lead SOIC_N | R-8 |
| OP249GSZ | −40°C to +85°C | 8-Lead SOIC_N | R-8 |
| OP249GSZ-REEL | −40°C to +85°C | 8-Lead SOIC_N | R-8 |
| OP249GSZ-REEL7 | −40°C to +85°C | 8-Lead SOIC_N | R-8 |

[1] Z = RoHS Compliant Part.

For military processed devices, see the standard microcircuit drawings (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp.

**Table 7.**

| SMD Part Number | Analog Devices, Inc. Equivalent |
|---|---|
| 5962-9151901M2A | OP249ARCMDA |
| 5962-9151901MPA | OP249AZMDA |

## NOTES

## NOTES

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