408-979

MOTOROLA

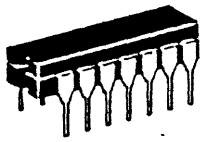
MC4344
MC4044

PHASE-FREQUENCY DETECTOR

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

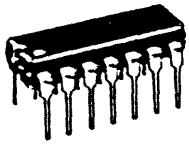
Operating Frequency = 8 MHz typ
Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

PHASE-FREQUENCY DETECTOR

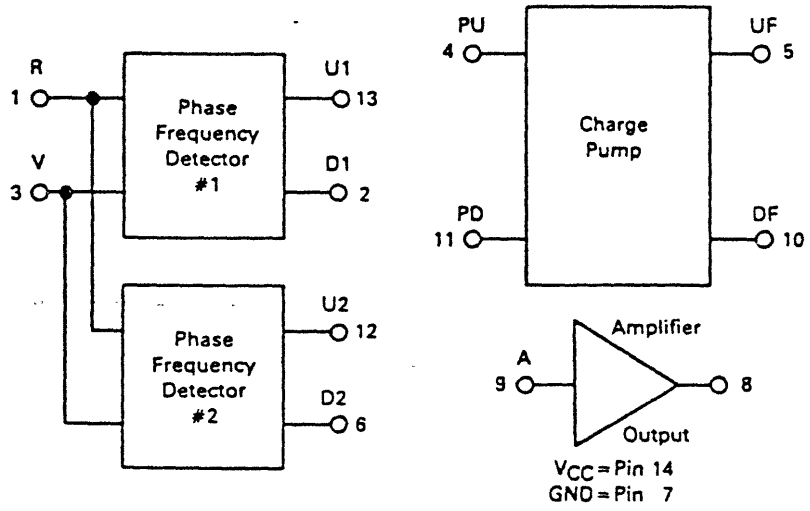


L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

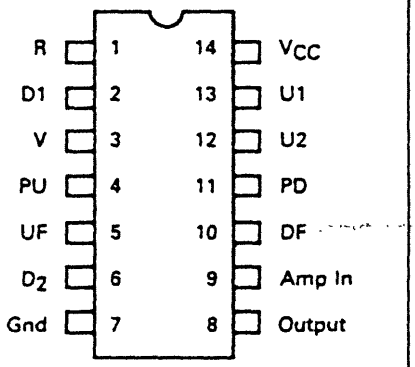
P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only



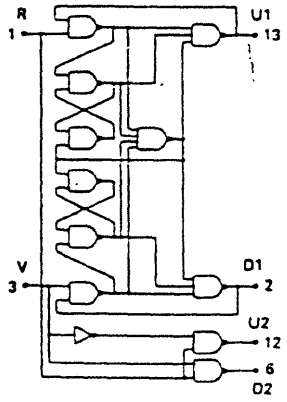
LOGIC DIAGRAM



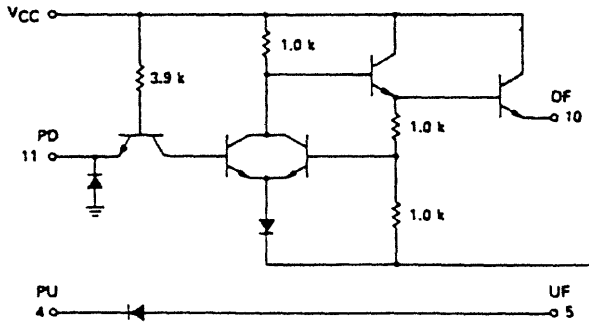
PIN ASSIGNMENT



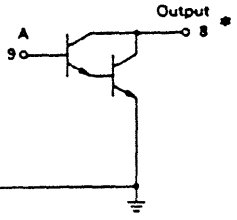
PHASE DETECTOR



CHARGE PUMP



AMPLIFIER



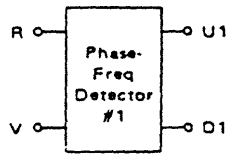
*V_{MAX} not to exceed 8.0 Vdc.

APPLICATION

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

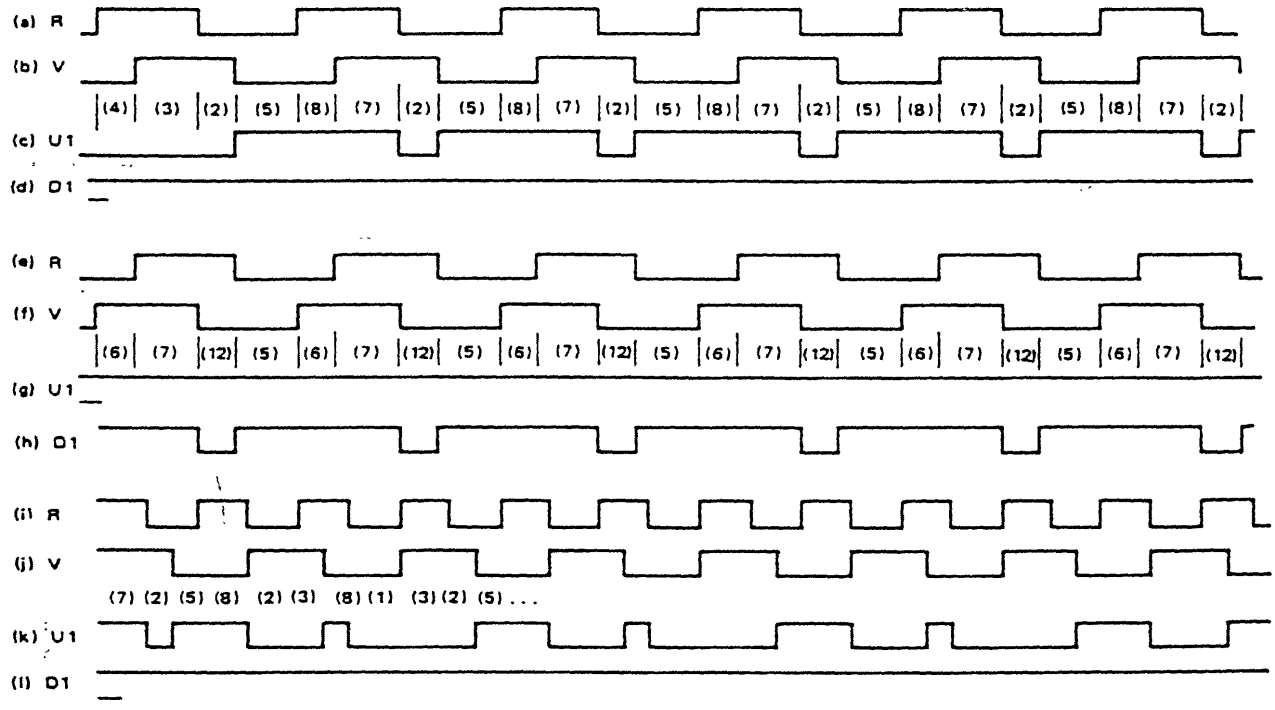
FIGURE 1 — PHASE DETECTOR #1 FLOW TABLE



R-V	R-V	R-V	R-V	U1	D1
0-0	0-1	1-1	1-0		
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
5	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

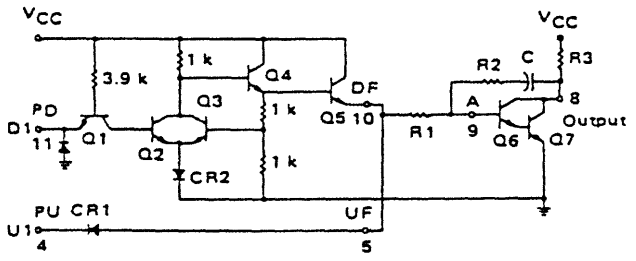
Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" an "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this

FIGURE 2 — PHASE DETECTOR #1 TIMING DIAGRAM



a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two V_{BE} drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be on V_{BE} below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

FIGURE 4 — CHARGE PUMP OPERATION

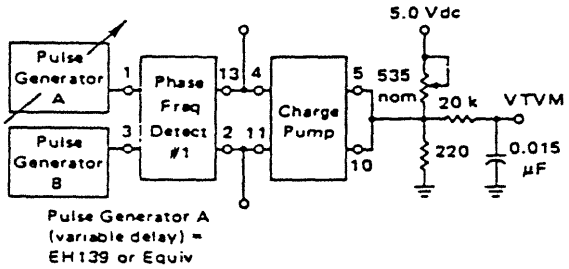


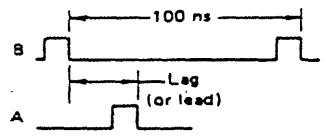
When PU is low and PD is high, CR1 is forward biased and UF will be approximately one V_{BE} above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one V_{BE} and three V_{BE} as the phase difference of R and V varies from minus 2π to plus 2π. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_ϕ, of approximately 0.12 volt/radian is obtained (see Figure 5).

The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects. The pump signals are established by V_{BE}s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower V_{BE}s — on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

FIGURE 5 — PHASE DETECTOR TEST





Shown for positive phase angle. Reverse A and B for negative phase angle.

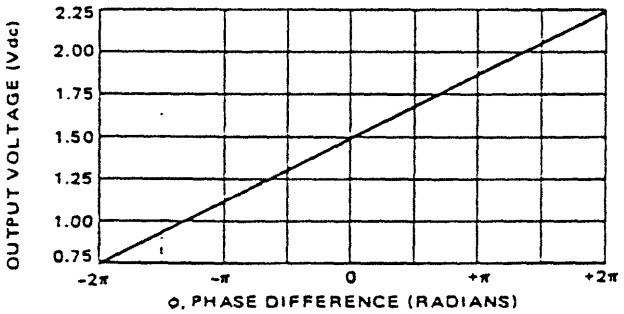
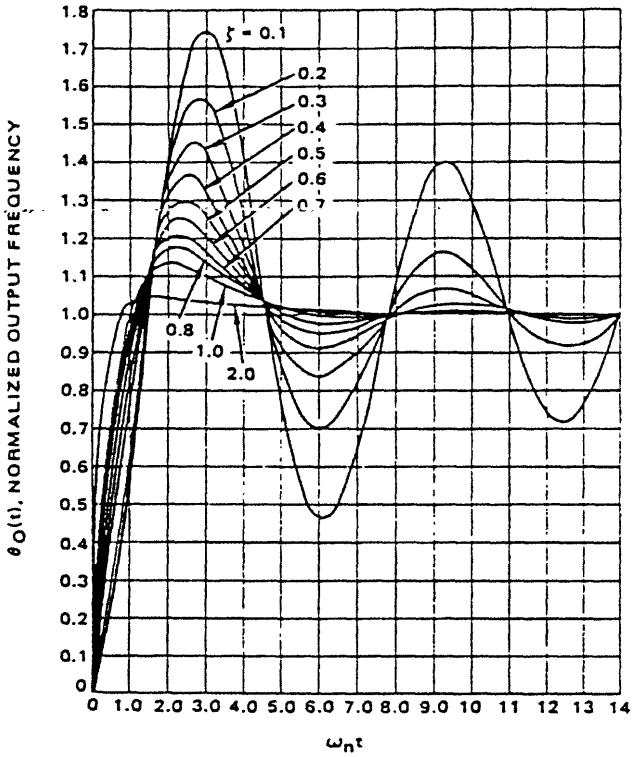


FIGURE 9 — TYPE 2 SECOND ORDER STEP RESPONSE



Using relationships 7 and 8, actual resistor values may be computed:

$$R_1 = \frac{K\phi K_V}{N\omega_n^2 C} \quad (9)$$

$$R_2 = \frac{2\zeta}{\omega_n C} \quad (10)$$

Although fundamentally the range of R_1 and R_2 may be from several hundred to several thousand ohms, sideband considerations usually force the value of R_1 to be set first, and then R_2 and C computed.

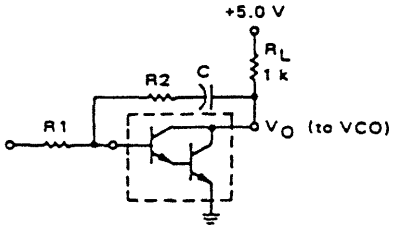
$$C = \frac{K\phi K_V}{N\omega_n^2 R_1} \quad (11)$$

Calculation of passive components R_2 and C (in synthesizers) is complicated by incomplete information on N, which is variable, and the limits of ω_n and ζ during that variance. Equally important are changes in K_V over the output frequency range. Minimum and maximum values of ω_n and ζ can be computed from Equations 4 and 5 when the appropriate worst case numbers are known for all the factors.

Amplifier/filter gain usually determines how much phase error exists between f_{in} and f_{out}, and the filter characteristic shapes capture range and transient performance. A relatively simple, low gain amplifier may usually be used in the loop since many designs are not constrained so much by phase error as by the need to make f_{in} equal f_{out}. Unnecessarily high gains can cause problems in linear loops when the system is out of lock if the amplifier output swing is not adequately restricted since integrating operational amplifier circuits will latch up in time and effectively open the loop.

The internal amplifier included in the MC4344/4044 may be used effectively if its limits are observed. The circuit configuration shown in Figure 10 illustrates the placement of R_1, R_2, C, and load resistor R_L (1 kΩ). Due to the non-infinite gain of this stage ($A_V \approx 30$) and other non-ideal characteristics, some restraint must be placed on passive component selection. Foremost is a lower limit on the value of R_2 and an upper limit on R_1. Placed in order of priority, the recommendations are as follows: (a) R2 > 50 Ω, (b) R1/R2 ≤ 10, (c) 1 kΩ < R1 < 5 kΩ.

FIGURE 10 — USING MC4344/4044 LOOP AMPLIFIER



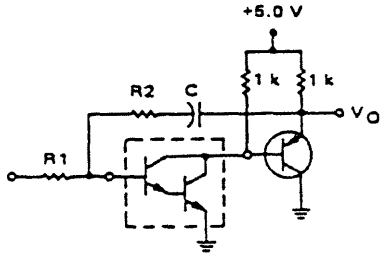
Limit (c) is the most flexible and may be violated with either higher sidebands and phase error (R_1 > 5 kΩ) or lower phase detector gain (R_1 < 1 kΩ). If limit (b) is exceeded, loop bandwidth will be less than computed and may not have any similarity to the prediction. For an accurate reproduction of calculated loop characteristics one should go to an operational amplifier which has sufficient gain to make limit (b) readily satisfied. Limit (a) is very important because T_1 in Equation 5 is in reality composed of three elements:

$$T_1 = C\left(R_2 - \frac{1}{g_m}\right) \quad (12)$$

where g_m = transconductance of the common emitter amplifier.

Normally g_m is large and T_1 nearly equals R_2C, but resistance values below 50 Ω can force the phase-compensating "zero" to infinity or worse (into the right half plane) and give an unstable system. The problem can be circumvented to a large degree by buffering the feedback with an emitter follower (Figure 11). Inequality (a) may then be reduced by at least an order of magnitude (R_2 > 5 Ω) keeping in mind that electrolytic capacitors used

FIGURE 11 — AMPLIFIER CAPABLE OF HANDLING LOWER R2



sizers with N > 1. However, a series of RC filters is not recommended for either extended pulse suppression or sideband improvement as excess phase will begin to build up at the loop crossover ($\approx \omega_n$) and tend to cause instability. This will be discussed in more detail later.

FIGURE 15 — IMPROVED TRANSIENT SUPPRESSION WITH R1 — C_c

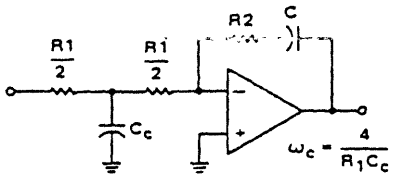
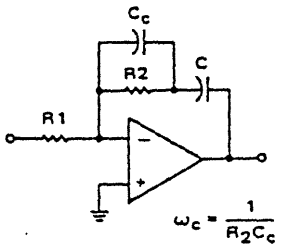


FIGURE 16 — IMPROVED TRANSIENT SUPPRESSION WITH R2 — C_c



Spurious Outputs

Although the major problem in phase-locked loop design is defining loop gain and phase margin under dynamic operating conditions, high-quality synthesizer designs also require special consideration to minimize spurious spectral components — the worst of which is reference-frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals — loop dynamic behavior, suppression of VCO noise, or suppression of other in-loop noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hardware is built.

Any steady-state signal on the VCO control will produce sidebands in accordance with normal FM theory. For small spurious deviations on the VCO, relative sideband-to-carrier levels can be predicted by:

$$\frac{\text{sidebands}}{\text{carrier}} \cong \frac{V_{ref} K_V}{2\omega_{ref}} \qquad (13)$$

where V_{ref} = peak voltage value of spurious frequency at the VCO input.

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop filter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components.

For the usual case where ω_{ref} is higher than $1/T_2$, the K_F function amounts to a simple resistor ratio:

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong -\frac{R_2}{R_1} \qquad (14)$$

By substitution of Equations 9 and 10, this signal transfer can be related to loop parameters.

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong \frac{2\zeta N\omega_n}{K_\phi K_V} = \frac{V_{ref}}{V_\phi} \qquad (15)$$

where V_{ref} = peak value of reference voltage at the VCO input, and
V_ϕ = peak value of reference frequency voltage at the phase detector output.

Sideband levels relative to reference voltage at the phase detector output can be computed by combining Equations 13 and 15:

$$\frac{\text{sideband level}}{f_{out}\text{ level}} = V_\phi \left(\frac{\zeta N\omega_n}{\omega_{ref} K_\phi}\right) \qquad (16)$$

From Equation 16 we find that for a given phase detector, a given value of R_1 (which determines V_ϕ), and given basic system constraints (N, f_{ref}), only ζ and ω_n remain as variables to diminish the sidebands. If there are few limits on ω_n, it may be lowered indefinitely until the desired degree of suppression is obtained. If ω_n is not arbitrary and the sidebands are still objectionable, additional filtering is indicated.

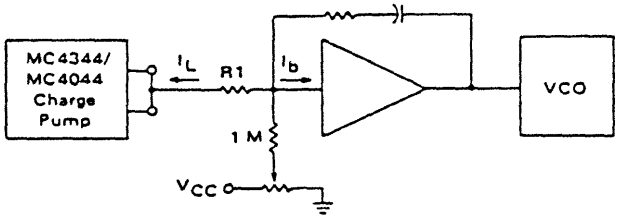
One item worthy of note is the absence of K_V in Equation 16. From Equation 15 it might be concluded that decreasing K_V would be another means for reducing spurious sidebands, but for constant values of ζ and ω_n this is not a free variable. In a given loop, varying K_V will certainly affect sideband voltage, but will also vary ζ and ω_n.

On the other hand, the choice of ω_n may well affect spectral purity near the carrier, although reference sideband levels may be quite acceptable.

In computing sideband levels, the value of V_ϕ must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves τ seconds

be achieved at a constant temperature. However when nulling fairly large values (> 100 nA), the rejection becomes quite sensitive since leakages are inherently a function of temperature. This technique has proved useful in achieving improved system performance when used in conjunction with good circuit practice and reference filtering.

FIGURE 19 — COMPENSATING FOR BIAS AND LEAKAGE CURRENT



Additional Loop Filtering

So far, only the effects of fundamental loop dynamics on resultant sidebands have been considered. If further sideband suppression is required, additional loop filtering is indicated. However, care must be taken in placement of any low pass rolloff with regard to the loop natural frequency (ω_n). On one hand, the "corner" should be well below (lower than) ω_{ref} and yet far removed (above) from ω_n. Although no easy method for placing the roll-off point exists, a rule of thumb that usually works is:

$$\omega_c = 5\omega_n \qquad (21)$$

Reference frequency suppression per pole is the ratio of ω_c to ω_{ref}.

$$SB_{dB} \cong n\ 20 \log_{10} \left(\frac{\omega_c}{\omega_{ref}}\right) \qquad (22)$$

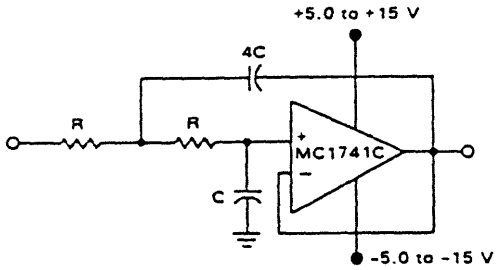
where n is the number of poles in the filter.

Equation 22 gives the additional loop suppression to ω_{ref}; this number should be added to whatever suppression already exists.

For non-critical applications, simple RC networks may suffice, but if more than one section is required, loop dynamics undergo undesirable changes. Loop damping factor decreases, resulting in a high percentage of overshoot and increased ringing since passive RC sections tend to accumulate phase shift more rapidly than signal suppression and part of this excess phase subtracts from the loop phase margin. Less phase margin translates into a lower damping factor and can, in the limit, cause outright oscillation.

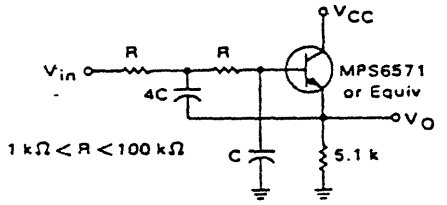
A suitable alternative is an active RC section, Figure 20, compatible with the existing levels and voltages. An active two pole filter (second order section) can realize a more gradual phase shift at frequencies less than the cutoff point and still get nearly equal suppression at frequencies above the cutoff point. Sections designed with a slight amount of peaking ($\zeta \cong 0.5$) show a good compromise between excess phase below cutoff (ω_c), without peaking enough to cause any danger of raising the loop gain for frequencies above ω_n. A fairly non-critical section may simply use an emitter follower as the active device with two resistors and capacitors completing the circuit (Figure 21). This provides a −12 dB/octave (−40 dB/decade) rolloff characteristic above ω_n, though the attenuation may be more accurately determined by Equation 22. If the sideband problem persists, an additional section may be added in series with the first. No more than two sections are recommended since at that time either (1) the constraint between ω_n and ω_{ref} is too close, or (2) reference voltage is modulating the VCO from a source other than the phase detector through the loop amplifier.

FIGURE 20 — OPERATIONAL AMPLIFIER LOW PASS FILTER



1. Choose R
   $1\ k\Omega < R < 1\ M\Omega$
2. $C = \frac{0.5}{\omega_c R}$

FIGURE 21 — EMITTER FOLLOWER LOW PASS FILTER

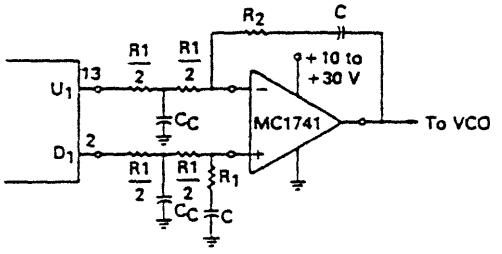


NOTE: If $V_O \geq V_{CC} - 1.0$ V, this stage is susceptible to power supply noise.

Operation without charge pump phase detector #1 of the MC4344/4044 can be implemented quite successfully in many applications without using the charge pump and internal darlington amplifier approach. An operational amplifier filter can be used to process the error information appearing at U1 and D1 (pins 13 and 2) directly (Figure 22). This phase detector/filter approach offers a potentially superior performing system because:

a. Charge pump delay time is eliminated.
b. Charge pump input signed threshold level need not be overcome before error information is obtained. This can result in a substantial improvement in the

FIGURE 22—TYPICAL FILTER AND SUMMING NETWORK



One solution to the ground-coupled noise problem is to lay out the return path with the most sensitive regulated circuit at the farthest point from power supply entry as shown in Figure 26.

Even for regulated subcircuits, accumulated noise on the ground bus can pose major problems since although the cross currents do not produce a differential load voltage directly, they do produce essentially common mode noise on the regulators. Output differential load noise then is a function of the input regulation specification. By far the best way to sidestep the problem is to connect each subcircuit ground to the power supply entry return line as shown in Figure 27.

FIGURE 26 — REGULATOR LAYOUT

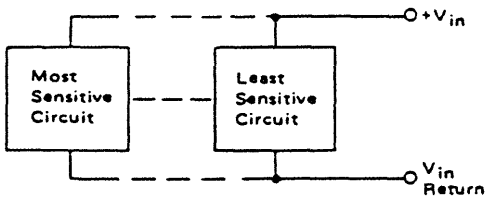
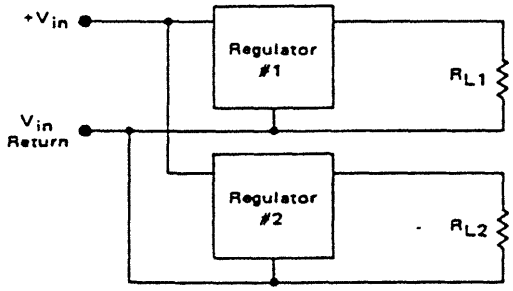


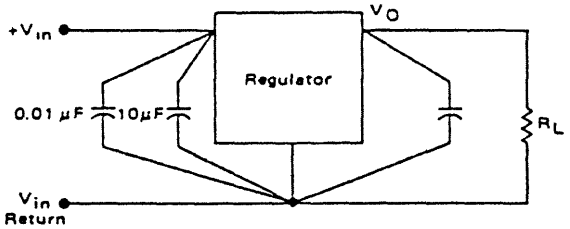
FIGURE 27 — REGULATOR GROUND CONNECTION



In Figures 25 and 27, R_{L1} and R_{L2} represent component groups in the system. The designer must insure that all ground return leads in a specific component group are returned to the common ground. Probably the most overlooked components are bypass capacitors. To minimize sidebands, extreme caution must be taken in the area immediately following the phase detector and through the VCO. A partial schematic of a typical loop amplifier and filter is shown in Figure 28 to illustrate the common grounding technique.

Bypassing in a phase-locked loop must be effective at both high frequencies and low frequencies. One capacitor in the 1.0-to-10 μF range and another between 0.01 and 0.001 μF are usually adequate. These can be effectively utilized both at the immediate circuitry (between supply and common ground) and the regulator if it is some distance away. When used at the regulator, a single electrolytic capacitor on the output and a capacitor pair at the input is most effective (Figure 29). It is important, again, to note that these bypasses go from the input/output pins to as near the regulator ground pin as possible.

FIGURE 29 — SUGGESTED BYPASSING PROCEDURE



APPLICATIONS INFORMATION

Frequency Synthesizers

The basic PLL discussed earlier is actually a special case of frequency synthesis. In that instance, $f_{out} = f_{in}$, although normally a programmable counter in the feedback loop insures the general rule that $f_{out} = Nf_{in}$ (Figure 30). In the synthesizer f_{in} is usually constant (crystal controlled) and f_{out} is changed by varying the programmable divider (÷ N). By stepping N in integer increments, the output frequency is changed by f_{in} per increment. In com-

FIGURE 30 — PHASE-LOCKED LOOP WITH PROGRAMMABLE COUNTER

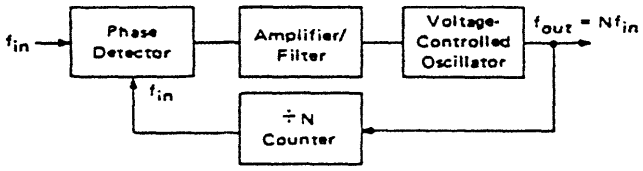
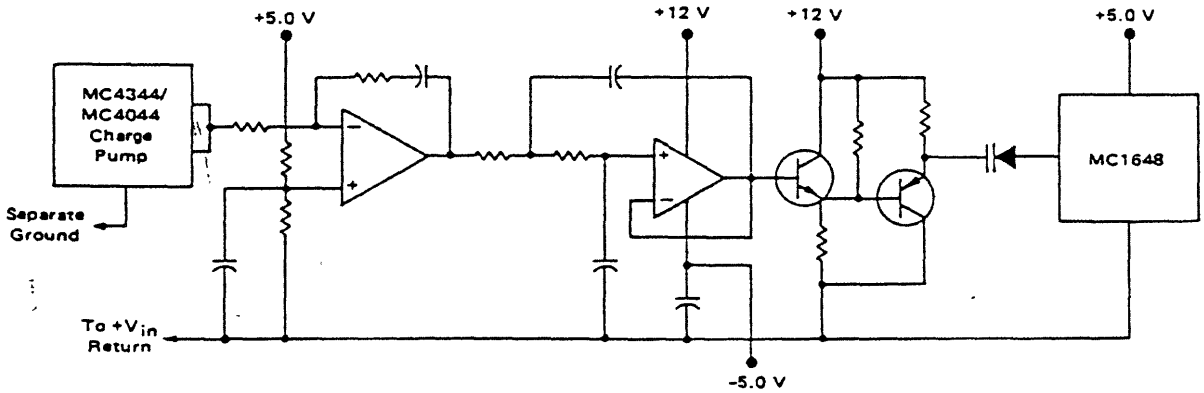


FIGURE 28 — PARTIAL SCHEMATIC OF LOOP AMPLIFIER AND FILTER



6. In order to compute C, phase detector gain and R1 must be selected. Phase detector gain, K_ϕ, for the MC4344/4044 is approximately 0.1 volt/radian with $R_1 = 1\ k\Omega$. Therefore,

$$C = \frac{(0.1)(11 \times 10^6)}{(30)(4.5 \times 10^3)^2(10^3)} = 1.8\ \mu F$$

7. At this point, R_2 can be computed:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C} = \frac{1.6}{(4.5 \times 10^3)(1.8 \times 10^{-6})} = 200\ \Omega$$

8. $$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}} = 0.98$$

9. Figure 9 shows that $\zeta = 0.98$ will meet the settling time requirement.
10. Sidebands may be computed for two cases: (1) with I_L (charge pump leakage current) nominal (100 nA), and (2) with I_L maximum (5.0 μA). A value of 5 μA will also be assumed for the amplifier bias current, i_b.

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{max} = \frac{(10 \times 10^{-6})(200)(11 \times 10^6)}{6.28 \times 10^5} \cong 35 \times 10^{-3}$$

The sideband-to-center frequency ratio nominally will be:

$$\left.\frac{\text{sideband}}{f_{out}}\right|_{nom} = \frac{5.1}{10} \times 35 \times 10^{-3}$$

$$= 20 \log_{10}(17.85 \times 10^{-3}) \cong -35\ dB$$

If desired additional sideband filtering can be obtained as noted in steps 11 and 12.

11. By splitting R_1 and C_C, further attenuation can be gained. The magnitude of C_C is approximately:

$$C_C = \frac{0.8}{R_1\omega_n} = \frac{0.8}{(10^3)(4.5)(10^3)} \cong 0.18\ \mu F$$

Improvement in sidebands will be:

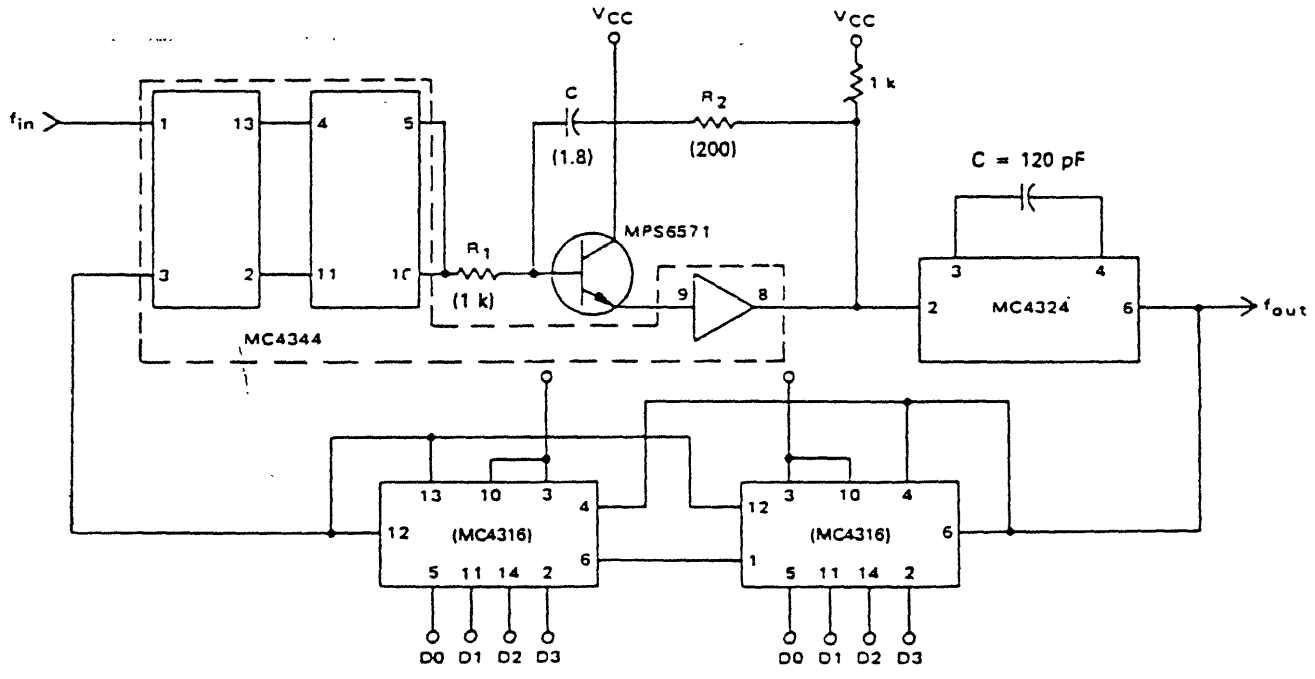
$$20 \log_{10} \frac{1}{\sqrt{1 + \frac{(2\pi \times 10^5)^2}{25(4.5 \times 10^3)^2}}} = -28\ dB$$

Nominal suppression is now −63 dB. Worst-case is 6 dB higher than nominal suppression of −57 dB. This is well within the −30 dB design requirement, step 12 is included for completeness only.

12. Attenuation of a second order filter is double that of the single order filter section described in step11. The calculations for a second order filter indicate an additional −56 dB of sideband rejection. Figures 20 and 21 show two second order filter configurations. If R is assigned a value of 10 kΩ then C may be calculated.

$$C = \frac{0.1}{\omega_n R} = \frac{0.1}{(4.5 \times 10^3)(10^4)} = 0.0022\ \mu F$$

FIGURE 31 — CIRCUIT DIAGRAM OF TYPE 2 PHASE-LOCKED LOOP



its complement, $\overline{DGATE}$, serve to initialize the circuitry and insure that the first transition of the data block (a phase transition) is ignored. The MC7493 binary counter and the G5-G12 latch generate a suitable signal for gating out G3 pulses caused by phase transitions at the end of a data cell, such as the one shown dashed in row 6.

The initial data pulse from G3 sets G12 low and is combined with DGATE in G7 to reset the counter to its zero state. Subsequent VCM clock pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state is decoded by G11, generating a negative transition. This causes G12 to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

Acquisition time is reduced if the loop is locked to a frequency approximately the same as the expected data rate during inter-block gaps. In Figure 32, this is achieved by operating the remaining half of the dual VCM at slightly less than the data rate and applying it to the reference input of the phase detector via the G8-G9-G10 data selector. When data appears, DGATE and $\overline{DGATE}$ cause the output of G3 to be selected as the reference input to the loop.

The loop parameters are selected as a compromise between fast acquisition and jitter-free tracking once synchronization is achieved. The resulting filter component values indicated in Figure 32 are suitable for recovering the clock from data recorded at a 120 kHz rate, such as would result in a tape system operating at 75 i.p.s. with a recording density of 1600 b.p.i. Synchronization is achieved by approximately the twenty-fourth bit time of the preamble. The relationship between system requirements and the design procedure is illustrated by the following sample calculation:

Assume a −3.0 dB loop bandwidth much less than the input data rate (≈ 120 kHz), say 10 kHz. Further, assume a damping factor of $\zeta = 0.707$. From the expression for loop bandwidth as a function of damping factor and undamped natural frequency, ω_n, calculate ω_n as:

$$\omega_{-3\,dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \quad (24)$$

or for $\omega_{-3\,dB} = (2\pi)10^4$ rad/s and $\zeta = 0.707$:

$$\omega_n = \frac{(2\pi)10^4}{2.06} = (3.05)10^4 \text{ rad/s}$$

As a rough check on acquisition time, assume that lockup should occur not later than half-way through a 40-bit preample, or for twenty 8.34 μs data periods.

$$\omega_n t = (3.05)10^4(20)(8.34)10^{-6} = 5.1 \quad (26)$$

From Figure 9, the output will be within 2 to 3% of its final value for $\omega_n t \approx 5$ and $\zeta = 0.707$. The filter components are calculated by:

$$\frac{K_\phi K_V}{R_1 C N} = \omega_n^2 \quad (27)$$

and

$$\frac{K_\phi K_V R_2}{R_1 N} = 2\zeta\omega_n \quad (28)$$

where $K_\phi = 0.115$ v/rad
$K_V = (18.2)\ 10^6$ rad/s/volt
$N = 24$ = Feedback divider ratio
$\omega_n = (3.05)\ 10^4$ rad/s
$\zeta = 0.707$

$$\frac{K_\phi K_V}{N} = \frac{(0.115)(18.2)10^6}{24} = (8.72)10^4$$

From Equation 27:

$$R_1 C = \frac{K_\phi K_V}{N\omega_n^2} = \frac{(8.72)10^4}{(3.05)^2 10^8} = (9.34)10^{-5}$$

From Equation 28:

$$\frac{R_2}{R_1} = \frac{2\zeta\omega_n N}{K_\phi K_V} = \frac{2(0.707)(3.05)10^4}{(8.72)10^4} = 0.494 \approx \tfrac{1}{2}$$

Let $R_1 = 3.0$ kΩ; then $R_2 = 1.5$ kΩ and

$$C = \frac{(9.34)10^{-5}}{(3.0)10^3} = (3.1)10^{-8}$$

or using a close standard value, use C = 0.033 μF. Now add the additional prefiltering by splitting R_1 and selecting a time constant for the additional section so that it is large with respect to R_2C_2.

$$10(\tfrac{1}{2}R_1)C_C = R_2C$$

or

$$C_C = \frac{2R_2C}{10R_1} = \frac{2(1.5)10^3(3.3)10^{-8}}{10(3.0)10^3} = 3300 \text{ pF}$$