

MGA-645T6

Low Noise Amplifier with Bypass/Shutdown Mode in Low Profile Package



Data Sheet

Description

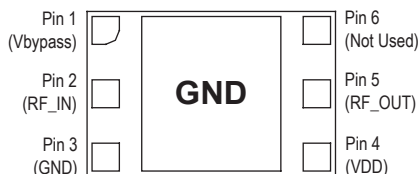
Avago Technologies' MGA-645T6 is an economical, easy-to-use GaAs MMIC Low Noise Amplifier (LNA) with Bypass/Shutdown mode. The LNA has low noise and high linearity achieved through the use of Avago Technologies' proprietary 0.5um GaAs Enhancement-mode pHEMT process. The Bypass/Shutdown mode enables the LNA to be bypassed during high input signal power and reduce current consumption. It is housed in a low profile 2 x 1.3 x 0.4mm 6-pin Ultra Thin Package. The compact footprint and low profile coupled with low noise, high linearity make the MGA-645T6 an ideal choice as a low noise amplifier for mobile receiver in the WiMax, WLAN(802.11b/g), WiBro and DMB applications.

Component Image



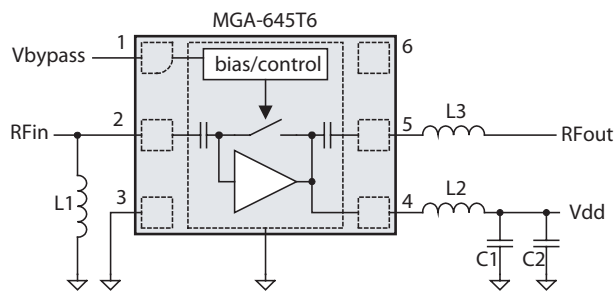
Note:
Package marking provides orientation and identification
"4F" = Product Code
"Y" = Year of manufacture
"M" = Month of manufacture

Pin Configuration



Top View

Simplified Schematic



Features

- 2.0 x 1.3 x 0.4 mm³ 6-lead Ultra Thin Package
- Low bias current
- Simple matching network
- 1.5 GHz – 3 GHz operating range
- Adjustable bias current
- Low Noise Figure
- Bypass/Shutdown Mode using a single pin
- Low current consumption in Bypass Mode, <100uA
- Fully matched to 50 ohm in Bypass Mode
- High Linearity (LNA and Bypass Mode)
- Low profile package

Typical Performance

2.4 GHz; 3V, 7mA (typ):

- 15 dB Gain
- 1.1 dB Noise Figure with 9dB Input Return Loss
- +7 dBm Input IP3
- -5 dBm Input Power at 1dB gain compression
- 4.5 dB Insertion Loss in Bypass Mode
- 16dBm IIP3 in Bypass Mode (Pin = -20dBm)
- <100uA current consumption in Bypass & Shutdown Mode

Applications

- Low noise amplifier for GPS, WiMax, WLAN, WiBro and DMB applications.
- Other ultra low noise applications in the 1.5 – 3 GHz band



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 60 V
ESD Human Body Model = 200 V
Refer to Avago Application Note A004R:
Electrostatic Discharge, Damage and Control.

Absolute Maximum Rating ^[1] TA=25°C

Symbol	Parameter	Units	Absolute Max.
V _{dd}	Device Voltage	V	4
V _{bypass}	Control Voltage	V	(V _{dd} -0.3)
P _{in,max}	CW RF Input Power	dBm	+15
P _{diss}	Total Power Dissipation ^[3]	mW	80
T _j	Junction Temperature	°C	150
T _{STG}	Storage Temperature	°C	-65 to 150

Thermal Resistance ^[2,3]

(V_{dd} = 3.0V, I_d=7mA), θ_{jc} = 60 °C/W

Notes:

1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Thermal resistance measured using Infra-Red Measurement Technique.
3. Board temperature T_B is 25 °C , for T_B >146 °C derate the device power at 14mW per °C rise in Board (package belly) temperature.

Product Consistency Distribution Charts ^[4]

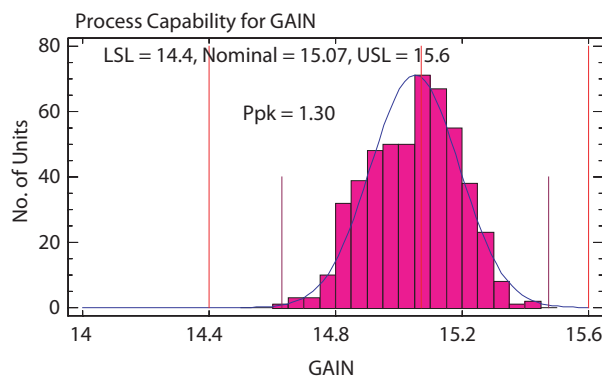


Figure 1. Gain @ 2.4 GHz , V_d 3V; V_{bypass} 1.8 V

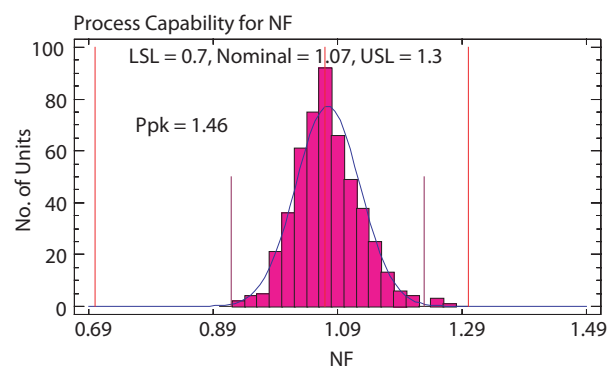


Figure 2. NF @ 2.4 GHz , V_d 3V; V_{bypass} 1.8 V

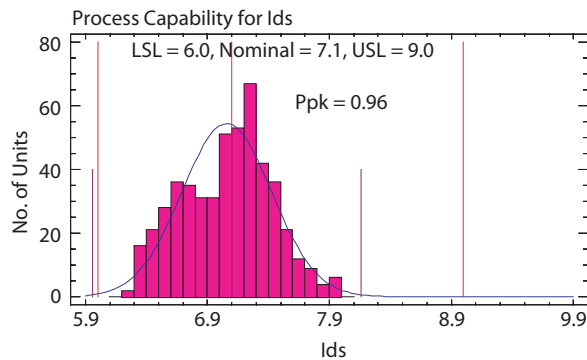


Figure 3. I_{ds} @ 2.4 GHz , V_d 3V; V_{bypass} 1.8 V

Notes:

4. Distribution data sample size are 500 samples taken from 3 different wafers and 3 different lots. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.

Electrical Specifications^[5,7]

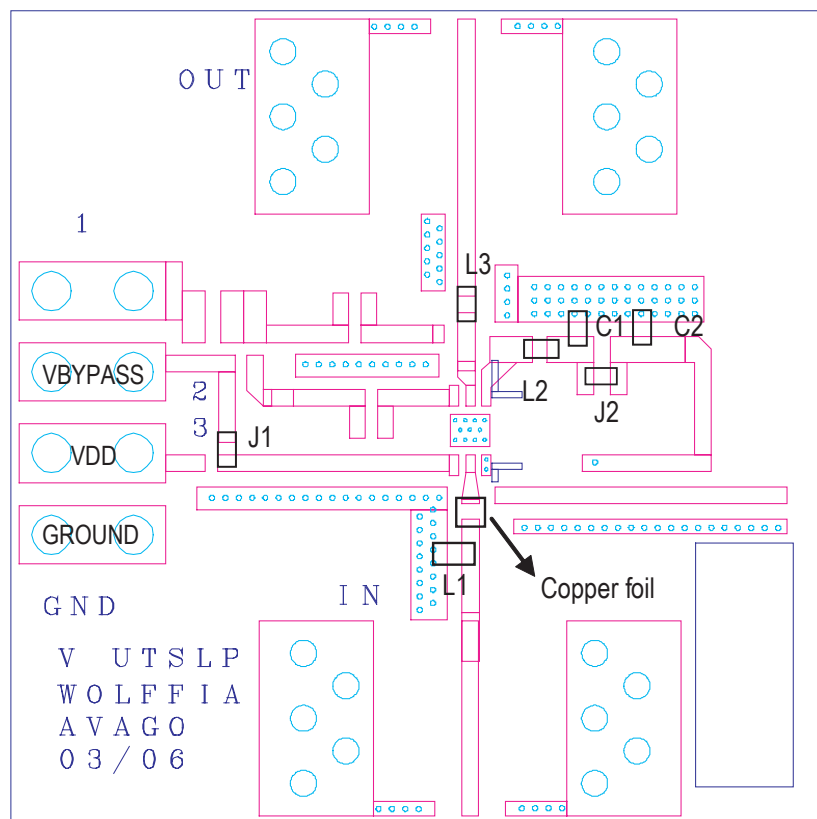
$T_A = 25\text{ }^\circ\text{C}$, $V_{dd} = 3\text{V}$, $V_{bypass} = 1.8\text{V}$, RF measurement at 2.4 GHz, measured on demo board (see Fig. 4) unless otherwise specified.

Symbol	Parameter and Test Condition	Units	Min.	Typ.	Max.
I_d	Bias Current	mA	-	7	13
Gain	Gain	dB	13.5	15	16.5
NF	Noise Figure (Typ. $V_{bypass} = 1.8\text{V}$)	dB	-	1.1	1.5
IIP3 ^[6]	Input Third Order Intercept Point	dBm	-	+7	-
OP1dB	Output Power at 1dB Gain Compression	dBm	-	+9	-
S11	Input Return Loss, 50 Ω source	dB	-	-9	-
S22	Output Return Loss, 50 Ω load	dB	-	-15	-
S12	Reverse Isolation	dB	-	-27	-
$ S_{21} _{2\text{BYPASS}}$	Bypass Mode Loss ($V_{bypass} = 0$)	dB	-	-4.5	-
IIP3 _{BYPASS}	Bypass Mode IIP3 (tested at -20dBm input Power)	dBm	-	16	-
$I_{d\text{BYPASS}}$	Bypass Mode current	μA	-	80	-

Notes:

- Measurements at 2.4GHz obtained using demo board described in Figure 1, with component values on Figure 2 (2.3 – 2.4 GHz)
- 2.4GHz IIP3 test condition: $F_{RF1} = 2.395\text{ GHz}$, $F_{RF2} = 2.4\text{ GHz}$ with input power of -30dBm per tone.
- Use proper bias, heatsink and derating to ensure maximum channel temperature is not exceeded. See absolute maximum ratings and application note for more details.

Demo Board Layout



*Application Notes: -

- Performance in a specified frequency band can be optimized by changing component values in the demoboard above to suit the application at that frequency. The schematic on page 4 and 7 show two sets of components used to demonstrate performance at the (2.3 - 2.4) GHz Wibro band and (2.5 - 2.7) GHz Wimax/DMB band.
- Operational Logic of Bypass/Shutdown pin (Pin 1)
 - Normal LNA operation : [1.2 to ($V_{dd}-0.3$)] Volt,
 - Bypass/Shutdown mode : 0 Volt or Open
 Pin 1 voltage in LNA mode can be varied to enable the LNA bias current to be adjusted, refer to next graph:

Figure 4. Demo Board Layout Diagram *

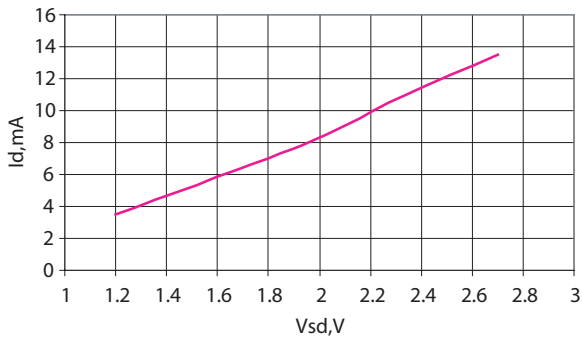
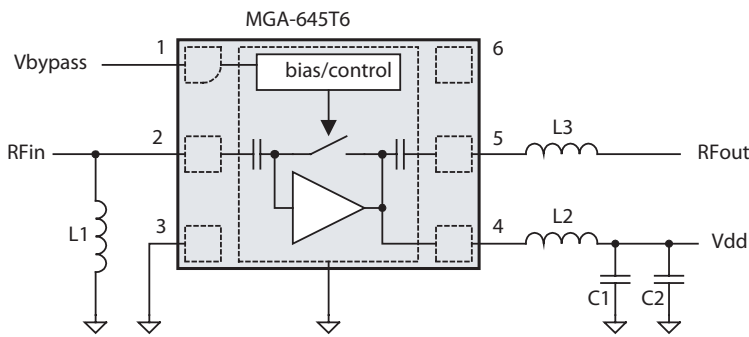


Figure 5. Id vs Vbypass (Vdd=3V)

Demo Board Schematic for 2.3–2.4 GHz tuning



Part	Size	Value	P/N
L1	0402	2.7nH	LL1005FH2N7B (TOKO)
L2	0402	3.9nH	LL1005FH3N9C (TOKO)
L3	0402	4.7nH	LL1005FH4N7C (TOKO)
C1	0402	11pF	MCH155A110JK(ROHM)
C2	0402	0.1uF	CM05X7R104K10AHF
J1,J2 ^[8]	0402	0 ohm	RK73Z1E000 (KOA)

Notes

8. Jumpers indicated in the demo board drawing are not needed in actual application board; this is because generic demo boards were used for development.

Figure 6. Demo Board Schematic Diagram

MGA-645T6 Typical Performance (2.3 – 2.4 GHz match)

TA = +25 °C, Vdd = 3V, Ids = 7mA (Vbypass = 1.8V), RF measurement at 2.4 GHz, Input Signal=CW unless stated otherwise.

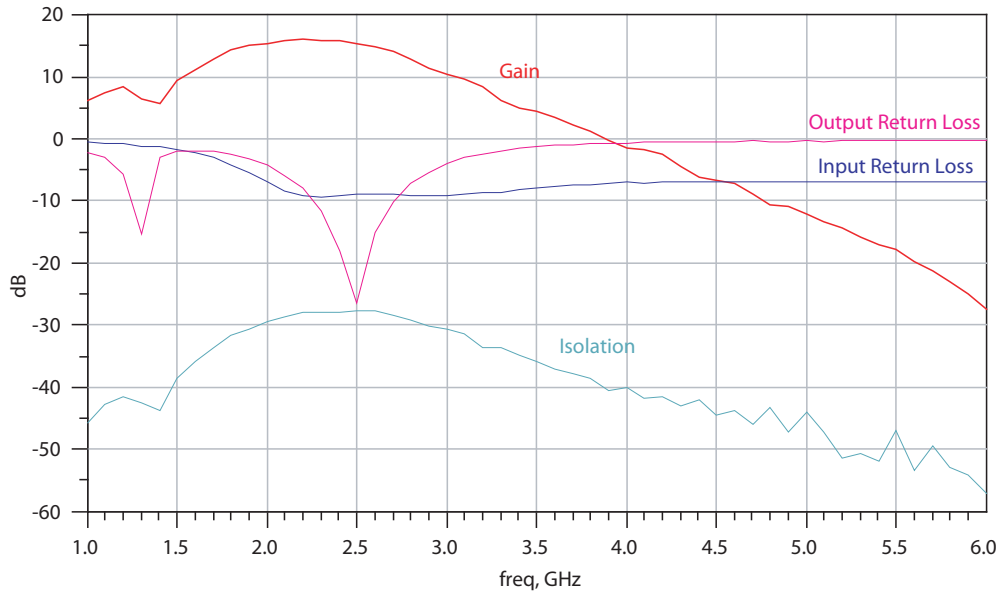


Figure 7. LNA Mode S21,S11,S22, S12 vs Frequency

LNA Mode Plots (2.3 – 2.4 GHz match) ; Vdd = 3V

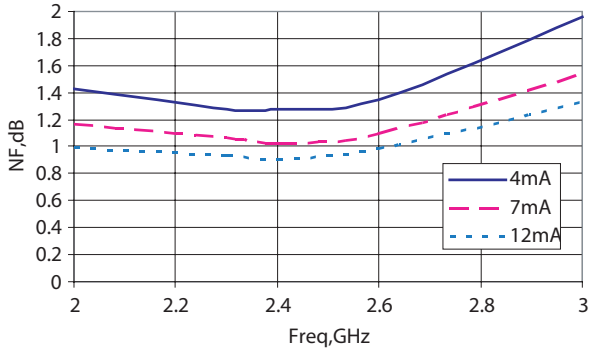


Figure 8. LNA Mode Noise Figure vs Frequency vs Id

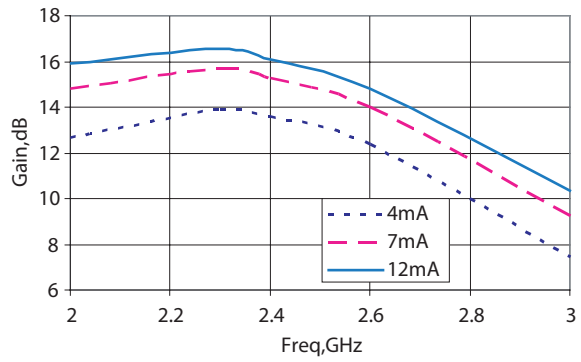


Figure 9. LNA Mode Gain vs Frequency vs Id

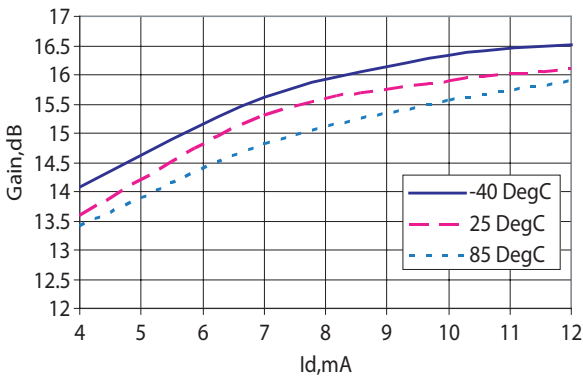


Figure 10. LNA Mode Gain vs Id vs Temperature

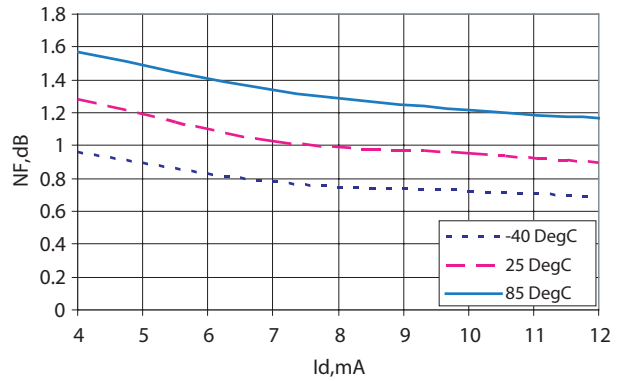


Figure 11. LNA Noise Figure vs Id vs Temperature

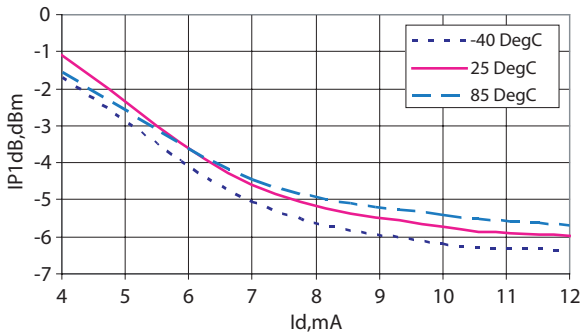


Figure 12. LNA Mode IP1dB vs Id vs Temperature

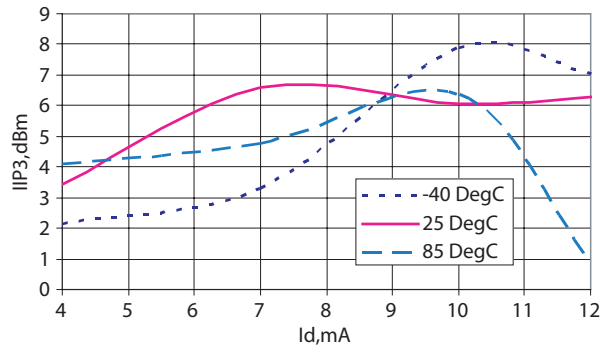


Figure 13. LNA Mode IIP3 vs Id vs Temperature

Bypass Mode Plots (2.3 – 2.4 GHz match) ($V_{dd} = 3V$; $V_{bypass} = 0V$)

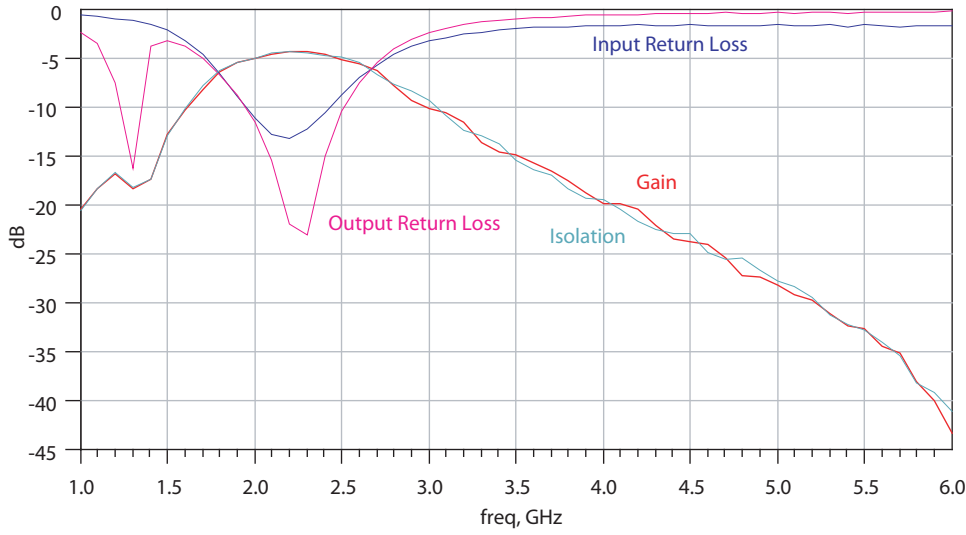


Figure 14. Bypass Mode S_{21} , S_{11} , S_{22} , S_{12} vs Frequency

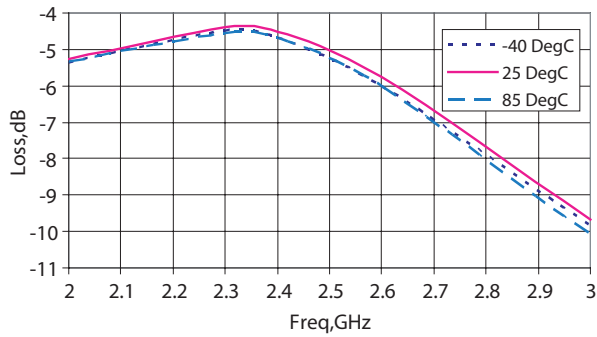


Figure 15. Bypass Mode Loss vs Frequency vs Temperature

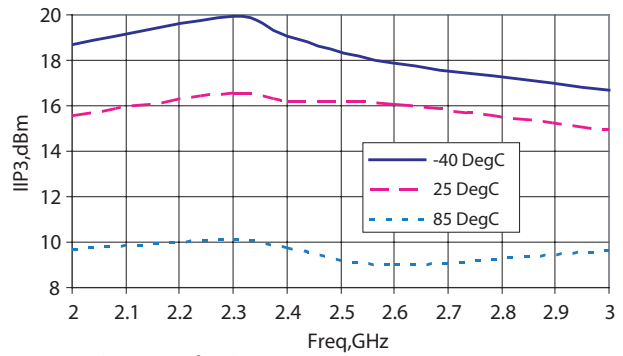


Figure 16. Bypass Mode IIP3 vs Frequency vs Temperature

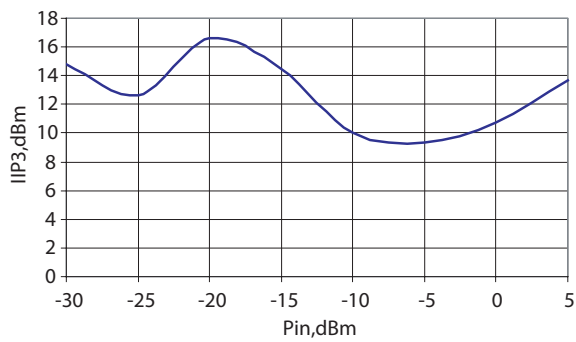
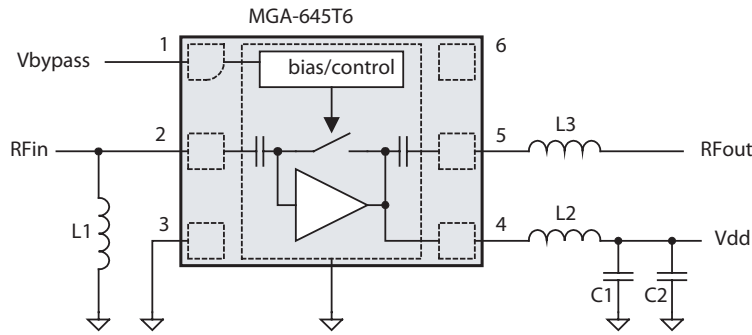


Figure 17. Bypass Mode IIP3 vs Input Power

Demo Board Schematic for 2.5 – 2.7 GHz tuning



Part	Size	Value	P/N
L1	0402	1.8nH	LL1005FH1N8B (TOKO)
L2	0402	3.9nH	LL1005FH3N9C (TOKO)
L3	0402	3.9nH	LL1005FH3N9C (TOKO)
C1	0402	11pF	MCH155A110JK(ROHM)
C2	0402	0.1uF	CM05X7R104K10AHF
J1,J2 ^[9]	0402	0 ohm	RK73Z1E000 (KOA)

Notes:

9. Jumpers indicated in the demo board drawing are not needed in actual application board; this is because generic demo boards were used for development.

Figure 18. Demo Board Schematic Diagram

MGA-645T6 Typical Performance (2.5 GHz – 2.7 GHz match)

TA = +25 °C, Vdd = 3V, Ids = 7mA (Vbypass = 1.8V), RF measurement at 2.6 GHz, Input Signal=CW unless stated otherwise.

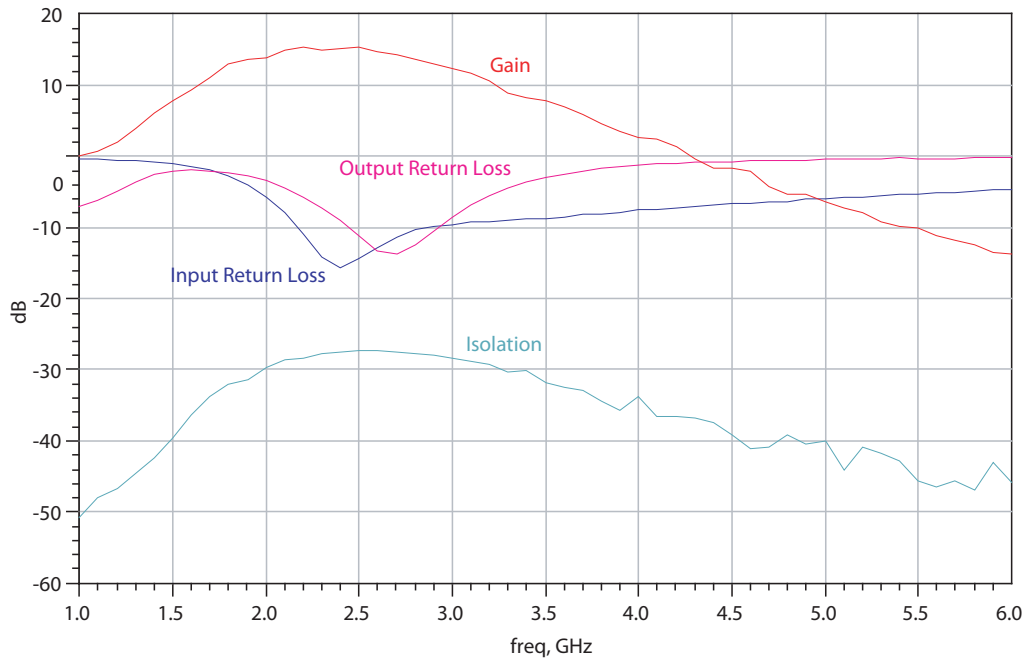


Figure 19. LNA Mode S21,S11,S22, S12 vs Frequency

LNA Mode Plots (2.5 – 2.7 GHz match) ; Vdd = 3V

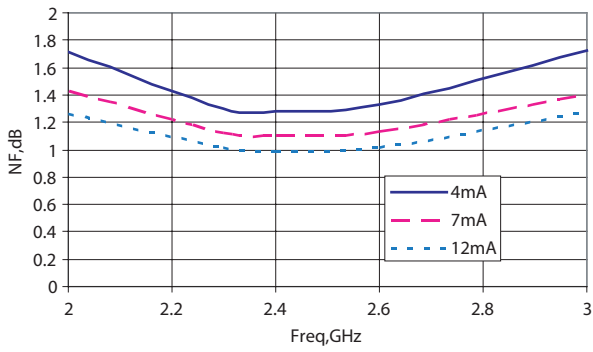


Figure 20. LNA Mode Noise Figure vs Frequency vs Id

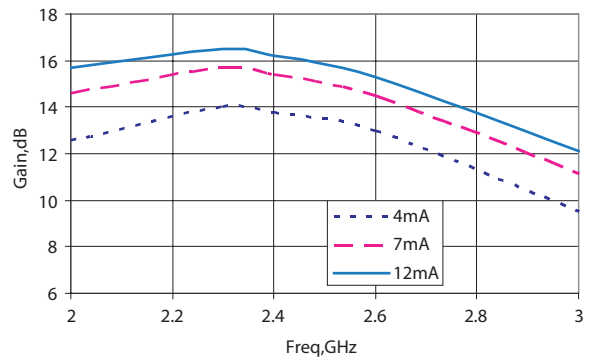


Figure 21. LNA Mode Gain vs Frequency vs Id

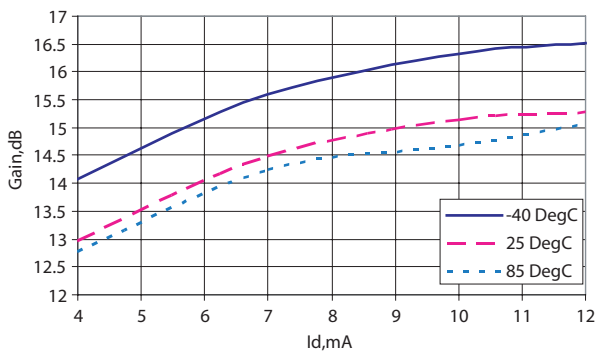


Figure 22. LNA Mode Gain vs Id vs Temperature

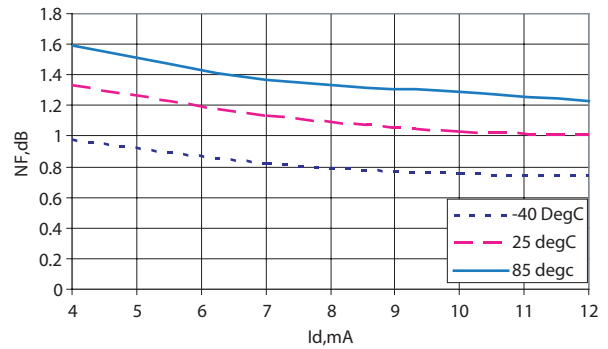


Figure 23. LNA Mode Noise Figure vs Id vs Temperature

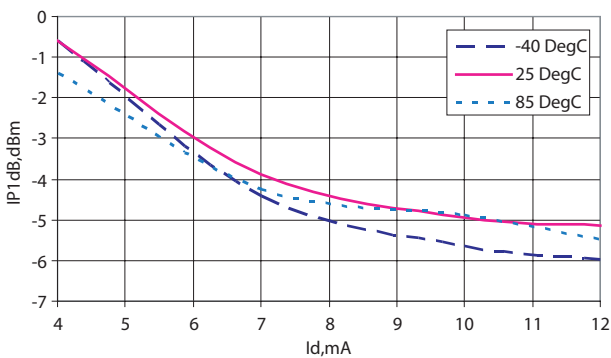


Figure 24. LNA Mode IP1dB vs Id vs Temperature

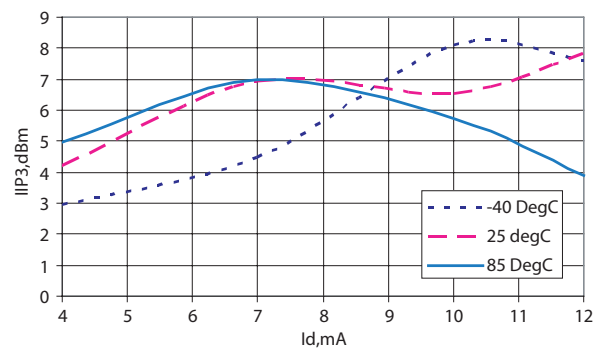


Figure 25. LNA Mode IIP3 vs Id vs Temperature

Bypass Mode Plots (2.5 – 2.7 GHz match) (Vdd=3V; Vbypass = 0V)

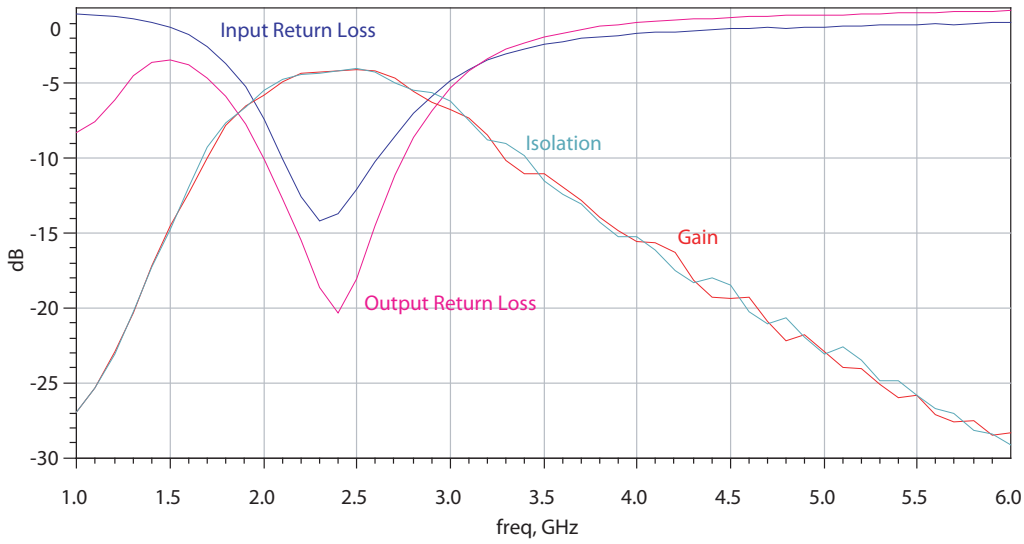


Figure 26. Bypass Mode S21, S11, S22, S12 vs Frequency

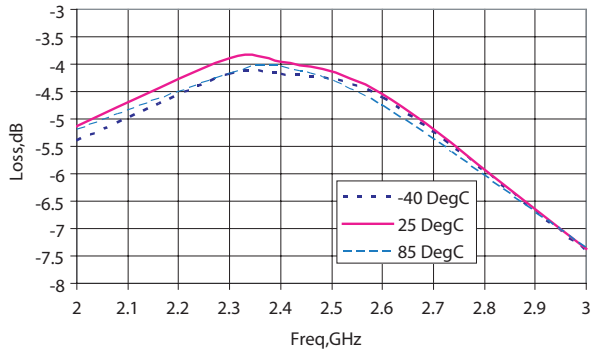


Figure 27. Bypass Mode Loss vs Frequency vs Temperature

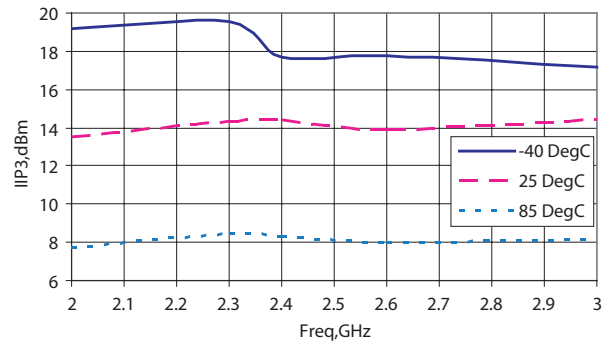


Figure 28. Bypass Mode IIP3 vs Frequency vs Temperature

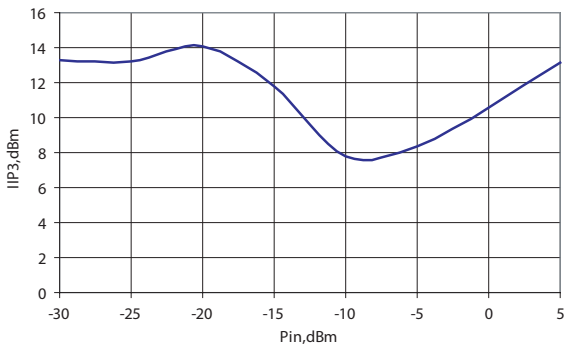
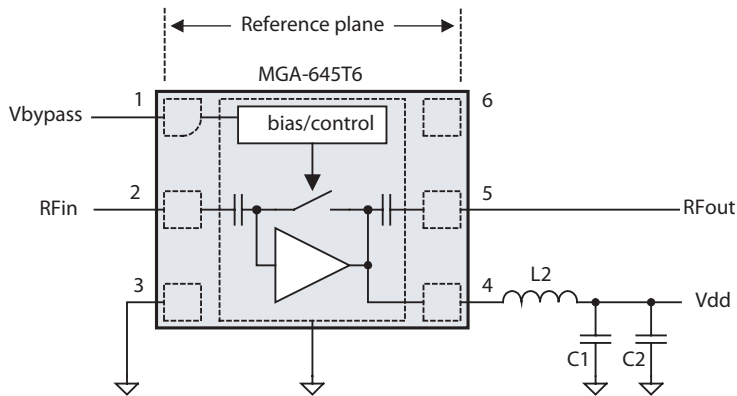


Figure 29. Bypass Mode IIP3 vs Input Power

Test Circuit For S and Noise parameter measurement^[10]



Part	Size	Value	P/N
L2	0402	3.9nH	LL1005FH3N9C (TOKO)
C1	0402	11pF	MCH155A110JK(ROHM)
C2	0402	0.1uF	CM05X7R104K10AHF

Note:

10. The measurement is calibrated up to the input (RFin) and output (RFout) pin of the package

Figure 30. S parameter and Noise parameter test circuit in an automated measurement system

MGA-645T6 LNA Mode typical scattering parameters at 25C, Vdd = 3V ; Id = 7mA

Freq. (GHz)	S11		S21			S12			S22	
	Mag	Ang	(dB)	Mag	Ang	(dB)	Mag	Ang	Mag	Ang
0.5	0.967	-24.335	7.88	2.4761	-75.33	-45.04	0.0056	-138.21	0.9085	-122.31
1	0.8861	-49.8342	13.58	4.7744	-171.657	-38.06	0.0125	128.9233	0.432	35.0635
1.5	0.8251	-69.8995	12.45	4.191	-157.794	-34.61	0.0186	156.2124	0.6571	85.1871
2	0.7269	-85.9353	11.73	3.8582	174.2387	-32.01	0.0251	132.069	0.6749	17.7274
2.1	0.7122	-88.7111	11.44	3.7313	171.389	-33.23	0.0218	130.7848	0.6811	10.4895
2.2	0.7006	-91.1084	11.21	3.6365	168.6844	-31.9	0.0254	128.8968	0.6819	4.1974
2.3	0.6845	-93.5463	11.01	3.5538	165.0165	-32.08	0.0249	127.6959	0.683	-2.0684
2.4	0.6713	-96.327	10.55	3.3705	161.92	-31.24	0.0274	127.563	0.6865	-7.48
2.5	0.6601	-98.4295	10.37	3.2988	161.3186	-31.4	0.0269	128.1856	0.691	-12.2626
2.6	0.6513	-100.828	10.23	3.246	159.714	-31.18	0.0276	130.7351	0.6867	-16.6168
2.7	0.6362	-102.875	9.99	3.1576	158.2845	-31.15	0.0277	128.1521	0.6901	-20.8737
2.8	0.6249	-105.268	9.53	2.9943	157.1203	-30.96	0.0283	124.8959	0.696	-24.8411
2.9	0.6152	-107.135	9.32	2.9234	156.0789	-31.7	0.026	132.4548	0.6926	-28.5477
3	0.6029	-108.961	8.95	2.8011	155.2783	-31.7	0.026	133.5121	0.6876	-32.1859
3.5	0.5491	-118.1	8.28	2.5942	151.9711	-30.49	0.0299	139.3989	0.6816	-49.8308
4	0.5013	-126.979	7.61	2.4026	146.6674	-30.2	0.0309	139.6368	0.6597	-70.0219
4.5	0.448	-136.942	6.63	2.1452	140.82	-29.55	0.0333	147.2432	0.6719	-93.7765
5	0.4005	-148.164	5.64	1.9149	135.5389	-29.82	0.0323	149.2084	0.6943	-118.882
5.5	0.3674	-160.461	4	1.5849	129.9475	-31.18	0.0276	154.87	0.7417	-139.598
6	0.3646	-175.708	2.14	1.279	125.6513	-30.75	0.029	162.4089	0.7978	-156.427
6.5	0.3856	169.0618	-0.11	0.9878	122.9896	-32.08	0.0249	166.7983	0.8348	-170.871
7	0.4261	155.8448	-2.91	0.7156	121.385	-35.97	0.0159	-177.345	0.8606	175.0569
7.5	0.4897	144.9997	-7.72	0.411	117.9594	-36.95	0.0142	-161.329	0.8771	157.9701
8	0.5128	139.1313	-20.71	0.0922	152.3853	-41.01	0.0089	-145.616	0.8565	136.2647
8.5	0.5981	138.3684	-8.88	0.3597	-97.8518	-36.89	0.0143	-61.0845	0.8059	106.3384
9	0.6552	135.8053	-1.62	0.8295	-110.242	-33.19	0.0219	-38.4428	0.7041	67.8904
9.5	0.6801	133.4826	1.94	1.2505	-124.174	-27.64	0.0415	-36.5714	0.5465	18.5069
10	0.6354	134.38	3.94	1.5743	-144.52	-25.9	0.0507	-72.2	0.3212	-48.88

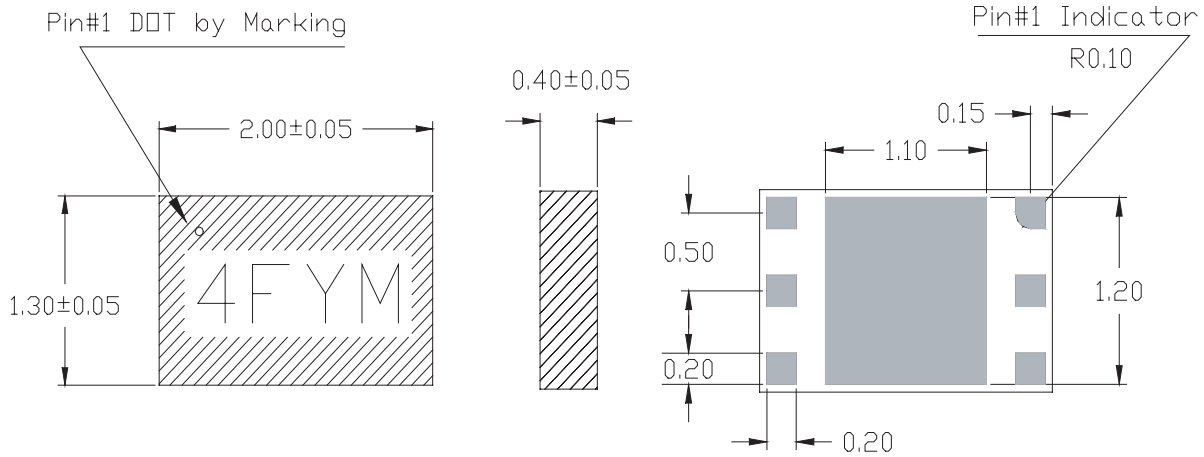
MGA-645T6 LNA Mode typical noise parameters at 25 °C, Vdd = 3V ; Id = 7mA

Freq.(GHz)	Fmin (dB)	Γ_{opt} Mag	Γ_{opt} Ang	Rn/50
2	0.55	0.76	67.8	0.23
2.1	0.57	0.76	71.04	0.22
2.2	0.59	0.75	74.29	0.21
2.3	0.62	0.75	77.54	0.21
2.4	0.72	0.69	79.72	0.2
2.5	0.75	0.68	82.9	0.2
2.6	0.78	0.67	86.08	0.2
2.7	0.8	0.66	89.11	0.19
2.8	0.83	0.65	92.14	0.18
2.9	0.85	0.63	95.17	0.18
3	0.88	0.62	98.2	0.17
3.1	0.91	0.61	100.88	0.16
3.2	0.95	0.6	103.56	0.16
3.3	0.98	0.59	106.24	0.15
3.4	1.02	0.58	108.92	0.14
3.5	1.06	0.57	111.6	0.14
3.6	1.09	0.56	114.08	0.13
3.7	1.12	0.56	116.56	0.13
3.8	1.15	0.55	119.04	0.12
3.9	1.18	0.55	121.52	0.12
4	1.21	0.54	124	0.11

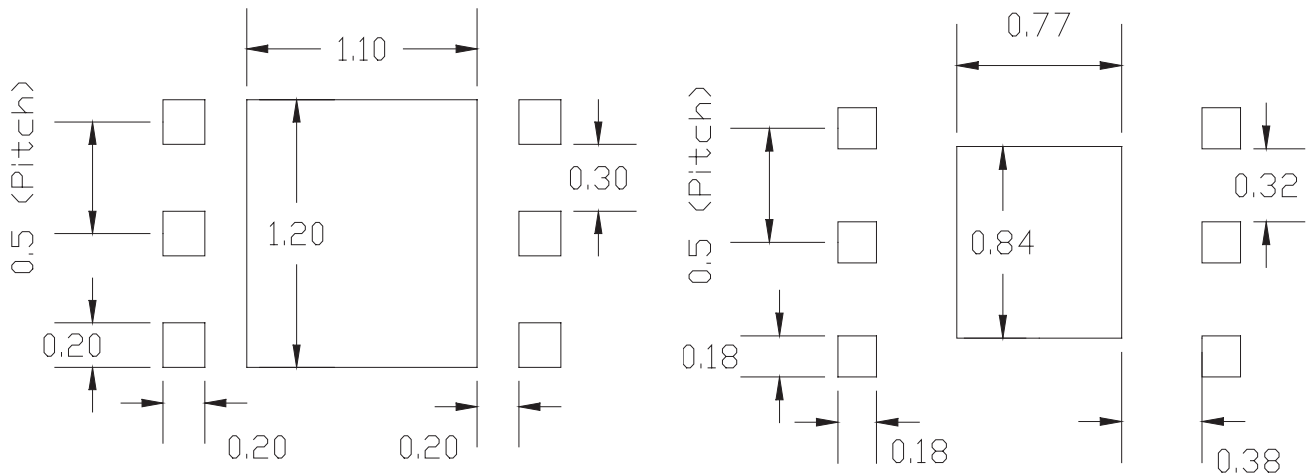
MGA-645T6 Bypass Mode typical scattering parameters at 25 °C, Vdd = 3V ; Vbypass = 0V

Freq. (GHz)	S11		S21			S12			S22	
	Mag	Ang	(dB)	Mag	Ang	(dB)	Mag	Ang	Mag	Ang
0.5	0.95	-31.2	-11.77	0.258	127.45	-11.77	0.258	125.95	0.568	111.9
1	0.925	-48.1	-10.96	0.283	100.5	-10.96	0.283	99.5	0.613	75.4
1.5	0.9	-65	-10.23	0.308	73.55	-10.23	0.308	73.05	0.658	38.9
2	0.875	-81.9	-9.55	0.333	46.6	-9.55	0.333	46.6	0.703	2.4
2.1	0.87	-85.28	-9.42	0.338	41.21	-9.42	0.338	41.31	0.712	-4.9
2.2	0.855	-88.66	-9.29	0.343	36.12	-9.29	0.343	36.22	0.722	-11
2.3	0.849	-91.44	-9.22	0.346	31.43	-9.22	0.345	31.63	0.734	-16.8
2.4	0.842	-94.52	-9.12	0.35	26.94	-9.12	0.349	27.14	0.741	-21.9
2.5	0.838	-97.2	-9.07	0.352	22.55	-9.07	0.352	22.65	0.741	-26.6
2.6	0.831	-100.18	-9	0.355	18.56	-9	0.354	18.76	0.749	-30.8
2.7	0.829	-102.56	-9	0.355	14.67	-9	0.356	14.77	0.745	-35.1
2.8	0.83	-105.14	-8.92	0.358	10.88	-8.92	0.358	10.98	0.74	-39.1
2.9	0.829	-107.52	-8.9	0.359	7.19	-8.9	0.359	7.39	0.739	-43
3	0.829	-109.9	-8.85	0.361	3.6	-8.85	0.361	3.8	0.73	-46.9
3.5	0.838	-120.9	-8.85	0.361	-12.35	-8.85	0.36	-12.15	0.69	-67
4	0.825	-130.8	-9	0.355	-27	-9	0.354	-26.7	0.694	-88.3
4.5	0.82	-139.2	-9.37	0.34	-41.85	-9.37	0.339	-41.65	0.717	-108.6
5	0.826	-148.4	-10.01	0.316	-56.6	-10.01	0.316	-56.4	0.74	-127.5
5.5	0.827	-161.3	-10.81	0.288	-71.55	-10.81	0.288	-71.55	0.778	-142.8
6	0.83	-176.4	-12.08	0.249	-84.4	-12.08	0.249	-84.2	0.829	-150.8
6.5	0.878	166.8	-13.76	0.205	-99.65	-13.76	0.204	-99.35	0.873	-160.3
7	0.895	154.4	-16.65	0.147	-114.9	-16.65	0.147	-114.7	0.893	-169.8
7.5	0.912	147	-21.21	0.087	-127.95	-21.21	0.087	-127.65	0.913	178.1
8	0.898	144.4	-33.56	0.021	-120.9	-33.56	0.021	-120.5	0.928	161.9
8.5	0.938	148.4	-22.38	0.076	-26.95	-22.38	0.076	-26.85	0.811	137
9	0.995	150.9	-22.05	0.079	-74.8	-22.05	0.08	-74.6	0.563	130.3
9.5	0.992	148.2	-32.77	0.023	-4.05	-32.77	0.023	-3.85	0.6	124.7
10	0.887	136.8	-15.34	0.171	8.8	-15.34	0.171	9.2	0.621	108.3

Package Dimensions

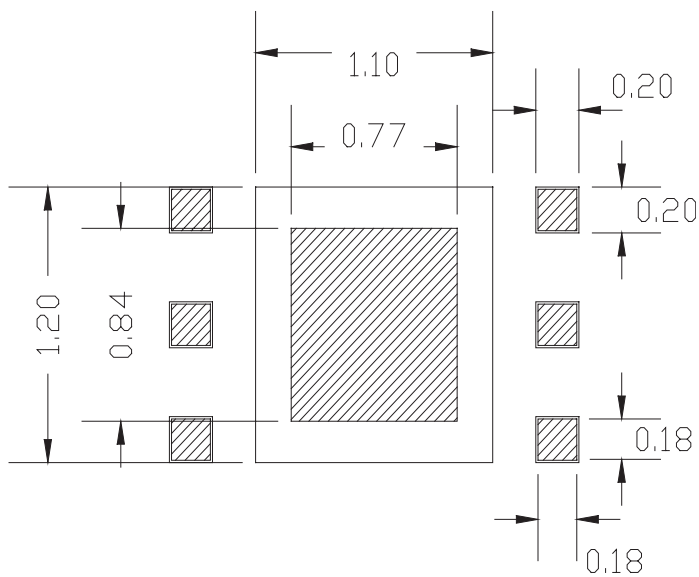


PCB Land Patterns and Stencil Design



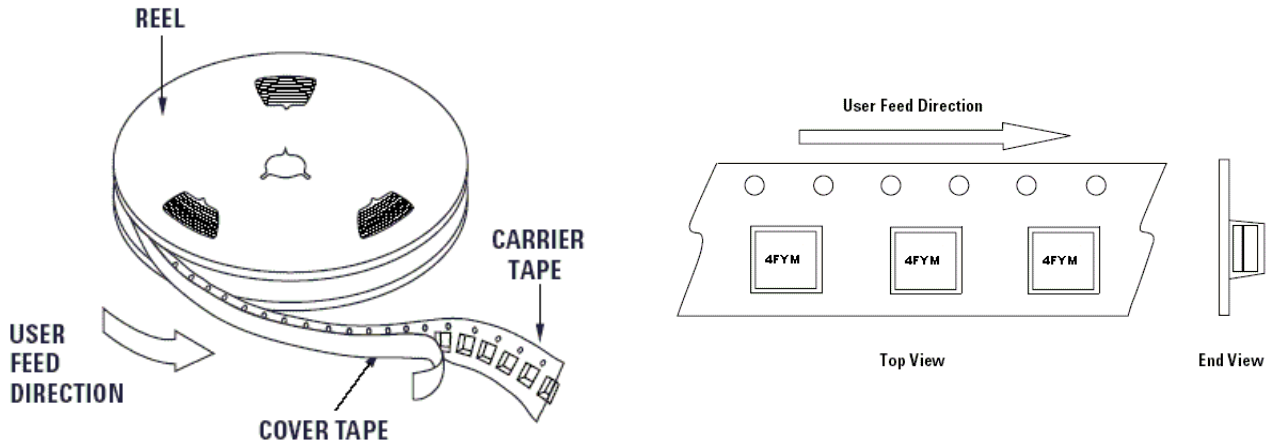
PCB Land Pattern (dimensions in mm)

Stencil Outline Drawing (dimensions in mm)

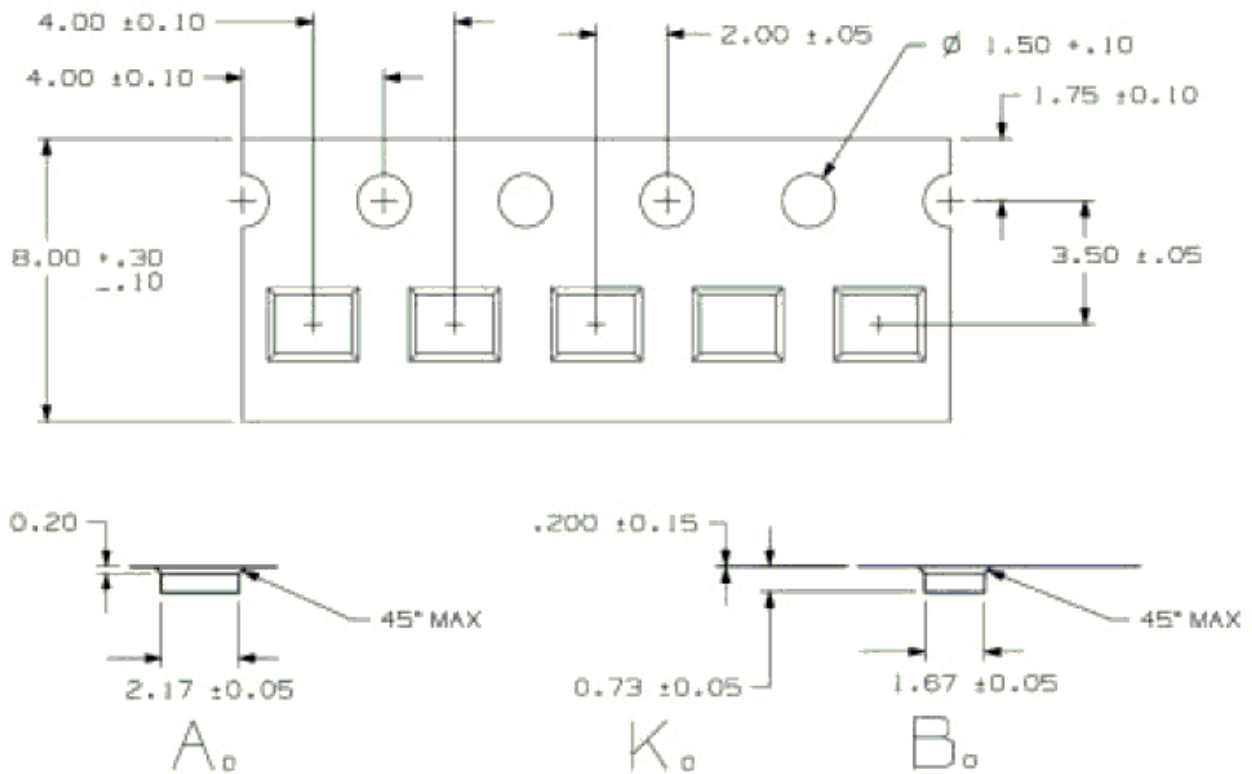


Combined PCB and Stencil Layouts (dimensions in mm)

Device Orientation



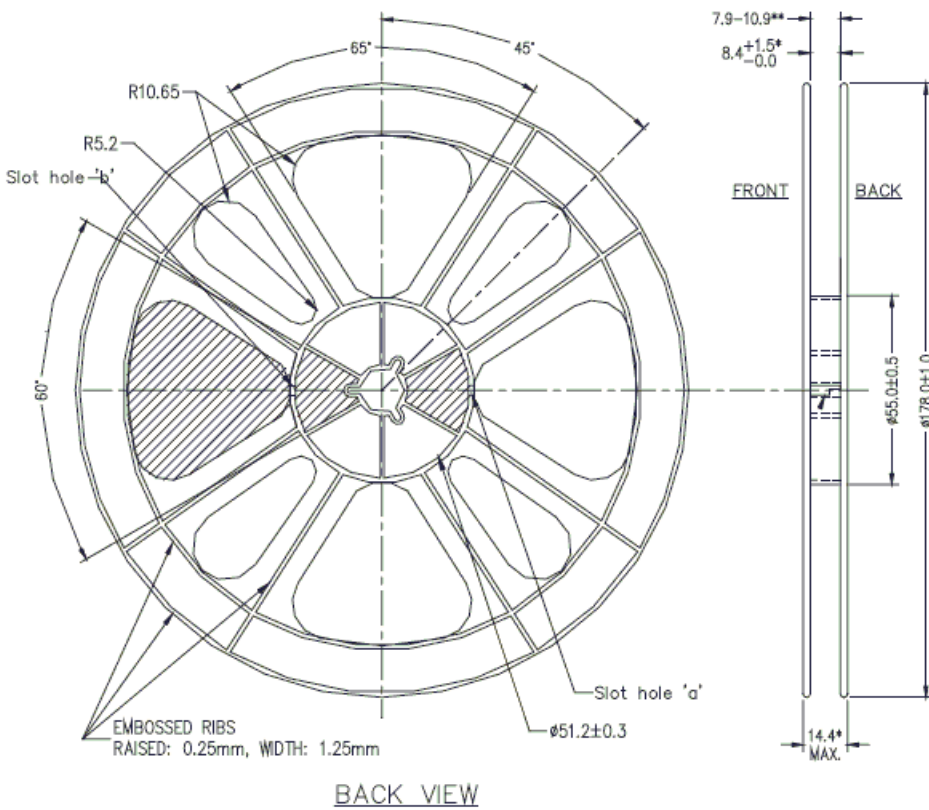
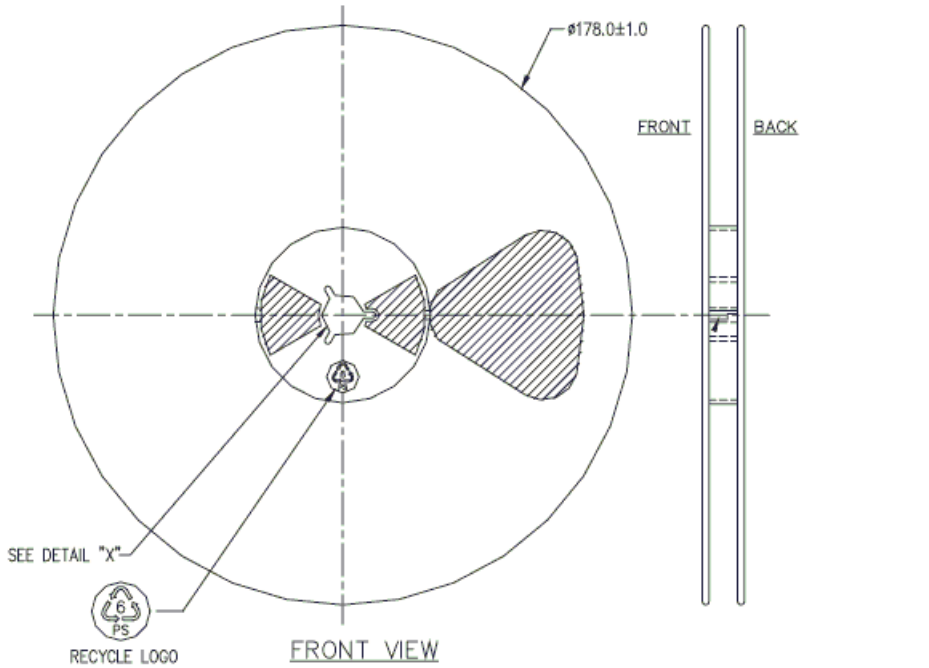
Tape Dimensions



Part Number Ordering Information

Part #	Qty	Container
MGA-645T6-BLKG	100	Antistatic Bag
MGA-645T6-TR1G	3000	7" Reel
MGA-645T6-TR2G	10000	13" Reel

Reel Dimensions



For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies, Limited in the United States and other countries. Data subject to change. Copyright © 2007 Avago Technologies Limited. All rights reserved. AV02-0006EN - January 30, 2007

