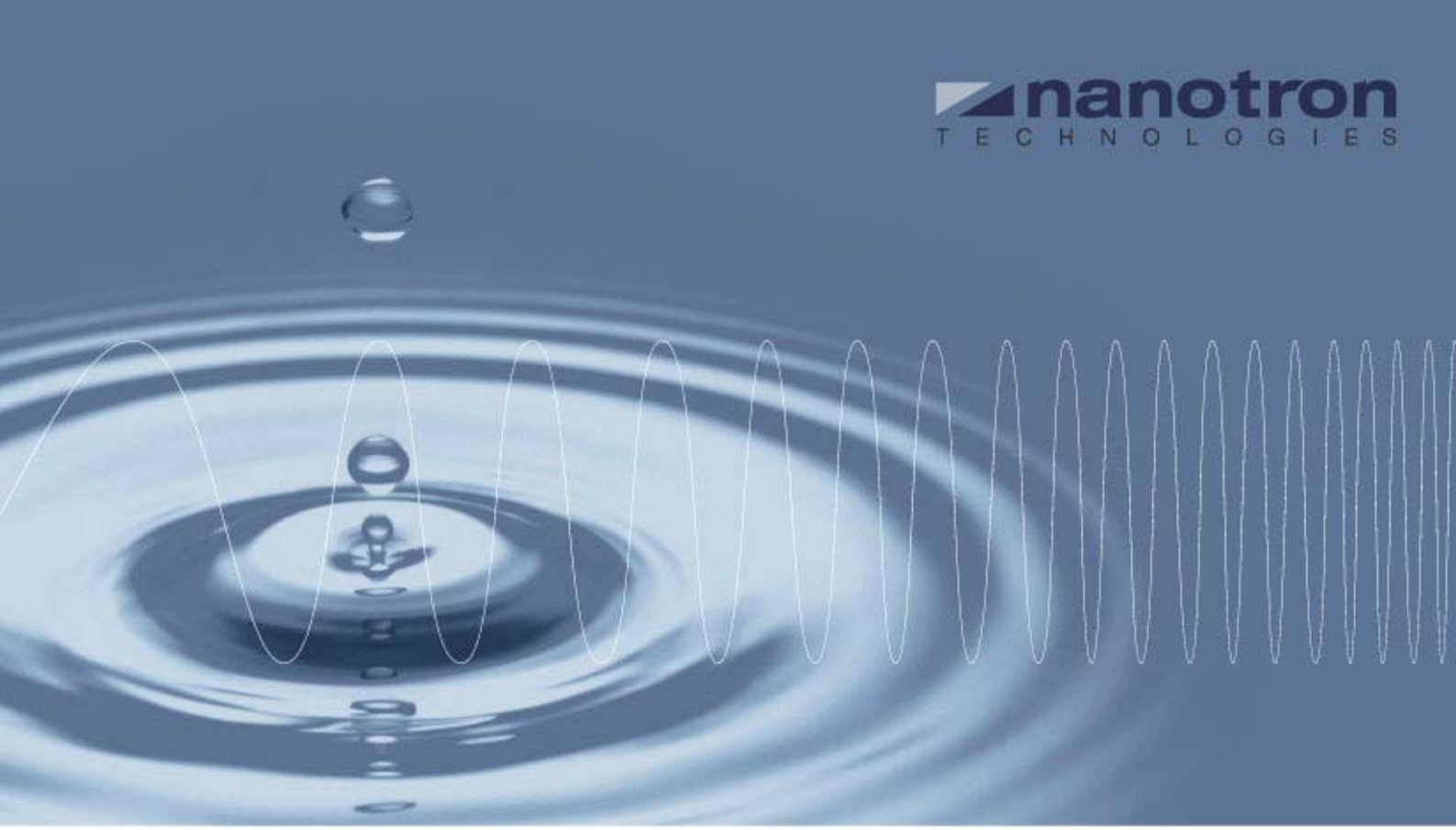

nanoNET TRX Transceiver (NA1TR8)

Datasheet

Version 2.08

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Chirp it.

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CAUTION! Electrostatic Sensitive Device. Precaution should be used when handling the device in order to prevent permanent damage.

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1 Product Summary

1.1 Description

The *nanoNET TRX Transceiver* is a highly integrated mixed signal chip utilizing a new wireless communication technology developed by *Nanotron Technologies GmbH – Chirp Spread Spectrum,* or simply CSS.

This innovative modulation technique permits the development of chips that have extremely low power consumption, operate over a wide range of temperatures, and perform effortlessly in robust wireless networks operating in the *2.45 GHz* ISM band.

The *nanoNET TRX Transceiver* offers an ideal solution for battery powered applications that require a reliable and extremely long operating lifetime, such as several years.

For communication over the air, CSS uses Upchirps and Downchirps with a symbol duration of T_{symbol} = *1 µs* and an effective bandwidth of B_{chirp} = *64 MHz*.

A wide variety of systems and applications can be developed with this novel technology, with the additional advantage of being able to select from data rates of either *500 kbps*, *1 Mbps,* or *2 Mbps*.

Conveniently, only a minimal number of external components are required to build a fully operational bi-directional communication node.

1.2 Key Features[1]

- Provides a single chip solution for a *2.45 GHz* ISM band RF transceiver
- Allows unregulated *2.4 V ... 3.6 V* supply voltage
- Includes an integrated SPI (slave mode only)
- Includes an integrated microcontroller management function
- Provides a maximum data rate of *2 Mbps*
- Provides a maximum range for LOS at *900 m* outdoors and *60 m* indoors (typical)
- Uses an effective chirp bandwidth of *64 MHz*
- Receiver sensitivity is *-92 dBm @ 1 Mbps*
- Carrier to Interference is *C/I = -3…0 dB @ C = -82 dBm*
- Processing gain is *17 dB*
- Current consumption is *35 mA* (RX), *78 mA* (TX) *@ 8 dBm*
- Standby current with active RTC is *1.5 µA*
- Allows an operating temperature range of between *-40° C* to *+85° C*
- Includes an integrated 4 channel digital I/O
- Includes an integrated MAC controller
- Provides a 32.768 kHz clock for microcontrollers
- Includes a programmable clock output at digital output

1.3 Applications

- Sensors and actors
- Manufacturing and logistics
- Active RFID
- Meter readers
- Building safety
- Medical applications
- Garage door openers
- Mouse, keyboards, and joysticks
- Home appliances
- Bell and door communication systems
- Baby phones

1. At nominal conditions, except otherwise specified. (See *Nominal Conditions* on page 2.)

1.4 Quick Reference Data

Table 1: Quick reference data

Parameter	Value	Unit
Minimum supply voltage	2.4	V
Maximum supply voltage	3.6	V
Maximum output power	8	dBm
Maximum data rate	2	Mbps
Sensitivity @ nominal conditions	-92	dBm
Supply current in transmit @ -15 dBm output power @ nominal conditions	58	mA
Supply current in transmit @ -5 dBm output power @ nominal conditions	64	mA
Supply current in receive mode @ nominal conditions	35	mA
Operating temperature range	-40 to +85	^{o}C
Supply current in Standby Mode with active RTC[a]	1.5	µA

a. *Under nominal conditions. See Nominal Conditions on page 2.*

1.5 Nominal Conditions

Nominal conditions are as specified below, except otherwise specified:

- Reference design (for measurement purposes only) has been used. See *Reference Design* on page 33.
- T_{junct} = 30° C
- $V_{SSA} = V_{SSD}$ = GND
- $V_{DDA} = V_{DDD}$ = 3.0 V
- Transmission/reception @ 1 Mbps and up/down chirp mode.
- Raw data mode: no CRC, no FEC, no encryption, no bit scrambling.
- BER = 0.001 during receive period.
- RF output power during transmit phase = 6.3 mW (+8 dBm) EIRP measured during continuous transmission.
- All RF ports are matched according to this specification.
- For range measurement, two identical *nanoNET* systems equipped with antennae representing 1.6 dBi gain have been used. Antennae with vertical E-polarization and omnidirectional horizontal radiation pattern have been used.
- Outdoor (open space) range measurement was performed on flat terrain, without vegetation higher than 0.2 m above ground, and without visible obstacles and other objects that could reasonably influence measurement results. Antennae for both *nanoNET* systems have been located 1.5 m above ground.
- Indoor range measurement was performed inside typical European office building where both nanoNET systems were located on the same floor.
- All RF powers (TX output power, RX sensitivity, etc.) are measured on the IC terminals (pins) under impedance matched conditions.

2 Abbreviations

µA	Microampere (unit of electrical current)
µC	Microcontroller
µCIrq	External microprocessor interrupt request
µCReset	External microprocessor reset
µCVcc	External microprocessor battery supply voltage
µCVccExt	External microprocessor power supply voltage
µF	Microfarad (unit of electrical capacitance)
µH	MicroHenry (unit of electrical resistance)
µs	Microseconds (unit of time)
Ω	Ohm (unit of electrical resistance)
Ack	Acknowledgement packet type
ADD	Actor/sensor
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
B	Battery
B	Frequency bandwidth
BA	Balun
BCH	Bose-Chaudhuri-Hochquenghem
BER	Bit Error Rate
BOM	Bill of Materials
bps	Bits per second (unit of data throughput)
C	Capacitor
C	Power of signal carrier
°C	Celsius (unit of temperature)
CCITT	Comité Consultatif International Téléphonique et Télégraphique
CDDL	Complementary Dispersive Delay Line
Clk	Clock
CRC	Cyclic Redundancy Check
CMMR	Common Mode Rejection Ratio
CS	Chip Select
CSMA	Carrier Sense Multiple Access
CSMA/CA	Carrier Sense Multiple Access/Collision Avoidance
CSS	Chirp Spread Spectrum
DAC	Digital to Analog Converter
Data	Data packet type
dB	Decibel (ratio between two values, such as signal power, voltage, or current levels in logarithmic scale)
dBi	Gain referenced to isotropic antennae
dBm	dB referenced to one milliwatt (10^{-3}W = 1mW)
DiIO	Digital Input/Output
DPA	Differential Power Amplifier
DPD	Differential Peak Detector
E_b	Energy of bit
EIRP	Effective Isotropic Radiated Power
FCD	Folded Chirp Detector
FCM	Folded Chirp Mixer
FEC	Forward Error Correction
FHSS	Frequency Hopping Spread Spectrum
FIFO	First In First Out
GHz	Gigahertz (unit of frequency)
GND	Ground
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IF	Intermediate Frequency
I_{OH}	Output current high
I_{OL}	Output current low
IRQ	Interrupt request
IQ	In-phase, Quadrature
ISM	Industrial Scientific Medical
ISO	International Organization for Standardization
kΩ	KiloOhms (unit of electrical resistance)
kHz	KiloHertz (unit of frequency)
kpbs	Kilobits per second (unit of data throughput)
L	Inductance
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MΩ	MegaOhms (unit of electrical resistance)
mA	Milliampere (unit of electrical current)
Mbaud	Megabauds
Mbps	Megabits per second (unit of data throughput)
MAC	Medium Access Control
MHz	MegaHertz (unit of frequency)
MISO	Master In, Slave Out
MIX	Mixer
MLF	Micro Lead Frame Package
MOD	Modulator
MOSI	Master Out Slave In
mW	milliwatt (unit of power)
NC	Not Connected
nF	Nanofarad (unit of electrical capacitance)
nH	NanoHenry (unit of electrical inductance)
N_o	Power spectral density of thermal noises
ns	Nanosecond (unit of time)
OSC	Oscillator
PAMP	Power amplifier
pF	Picofarad (unit of electrical capacitance)
ppm	parts per million
PCB	Printed Circuit Board
PGC	Power Gain Control
POMD	Peak Over Mean Detector
R	Resistor
RF	Radio Frequency
RFID	Radio Frequency IDentification
RSSI	Radio Signal Strength Indicator
RTC	Real Time Clock
RX	Receiver
S	Switch/button
SAW	Surface Acoustic Wave
SLNA	Symmetric Low Noise Amplifier
SMIX	Symmetric Mixer
SPI	Serial Peripheral Interface
SpiClk	Serial peripheral interface Clock
SpiSsn	Serial peripheral interface Slave select
SpiRxD	Serial peripheral interface Receive Data
SpiTxD	Serial peripheral interface Transmit Data
t	Time constant
T	Duration time of the chirp waveform
TBD	To Be Determined
TDMA	Time Division Multiple Access
T_{junct}	Temperature of junction
TRX	Transceiver
TX	Transmitter
V	Volts (unit of electrical potential)
V_{IH}	Input voltage for High level
V_{IL}	Input voltage for Low level
V_{OH}	Output voltage for High level
V_{OL}	Output voltage for Low level
V_{CC}	Battery supply voltage
VCO	Voltage Controlled Oscillator
V_{DDA}	Power supply for analog part
V_{DDD}	Power supply for digital part
VFQFPN	Very thin Fine pitch Quad Flat Pack Nolead Package
VGA	Variable Gain Amplifier
V_{SSA}	Analog ground
V_{SSD}	Digital ground
VSWR	Voltage Standing Wave Ratio
XTAL	Crystal

3 General Description

The *nanoNET TRX IC* is a fully integrated transceiver consisting of:

- a complete analog receiver (from antenna input to the demodulated digital data output).
- a complete transmitter (from digital data input to RF power amplifier output which can be directly connected to the antenna input) with additional support for an external power transistor. An external transistor or amplifier can boost transmission power from, for example, *+8 dBm* to *+20 dBm* (6.3 *mW* to *100 mW* respectively).
- a programmable digital controller communicating with an external microcontroller via a serial peripheral interface (SPI). This controller incorporates a baseband controller and a Medium Access Controller (MAC). The baseband controller performs the processing of data (framing, error correction, en/decryption, and so on) while the MAC controller applies CSMA/CA, TDMA or hybrid-access schemes for medium access.

Using CSS, this chip produces Upchirps and Downchirps with a symbol duration of T_{symbol} = *1µs* and an effective frequency bandwidth of B_{chirp} = *64 MHz*. CSS enables the development of different systems where application software can select physical data rates of *500 kbps, 1 Mbps,* or *2 Mbps*.

This IC is designed in such a way that only a minimum number of external elements are required to develop a fully operational bi-directional wireless communication node.

Even very slow microcontrollers can work together with this high speed transceiver, due to its use of FIFOs (First In, First Out).

The *nanoNET TRX Transceiver* provides two buffers (a 1024 bit receive buffer and a 1024 bit transmit buffer) dedicated to storing the payload of either received packets or ready to be transmitted data packets. These buffers can be accessed independently of each other – the receive buffer can receive data from the antenna while the transmit buffer can simultaneously be filled with data for the next packet transmission.

A programmable support block is provided, which consists of a real time clock, wake up circuitry, power management, low battery voltage measurement, and several adjustment and calibration functions for the analog part of the transceiver.

The digital IO pin number 4 (DilO4) on the chip provides a 32.768 kHz clock for use by an external microcontroller on chip startup. It can be switched off after power up if not needed or it can be programmed to operate in another frequency (32.768 kHz or from 125 kHz to 16 MHz). Furthermore, the three other digital IO pins (DilO1, DilO2, DilO3) provided by the chip can also be programmed to operate in a frequency in the same range as DilO4.

Moreover, all important functions of this block can be setup and controlled by an application software. A *Receive Signal Strength Indicator* (RSSI) is also provided, which can be supported and controlled by the application. This RSSI value is required when CSMA is implemented and can be used, for example, to indicate when the air interface is free or busy.

The bit processing methods of the *nanoNET TRX* include:

- Scrambling
- CRC (Cyclic Redundancy Check) generation and checking (CRC types include: ISO/IEC3309, CCITT X.25, X.75, ETS 300 125 / IEC 60870-5-1 / CCITT-32)
- 128 bit encryption/decryption (stream cipher with support of one time pads)
- FEC (forward error correction) block coded

Scrambling, encryption/decryption, and FEC can be enabled by the application, while the CRC type is selectable.

Transmission power can be programmed by the application and can be reduced in steps (from maximum *+8 dBm*) in a range of *Gain* ≥ *35 dB*. This means that the transmission power can vary from *-27 dBm* to *+8 dBm* without any additional external power amplifier or attenuator.

The sensitivity of the *nanoNET TRX Transceiver* is defined by the raw data mode (data not coded or encrypted in anyway) where *BER = 0.001*. Sensitivity is $P_{sensitivity}$ = *-92 dBm* or better. For an isotropic antenna, link budget is equal to A_{link_budget} = 100 dB.

4 Block Diagram

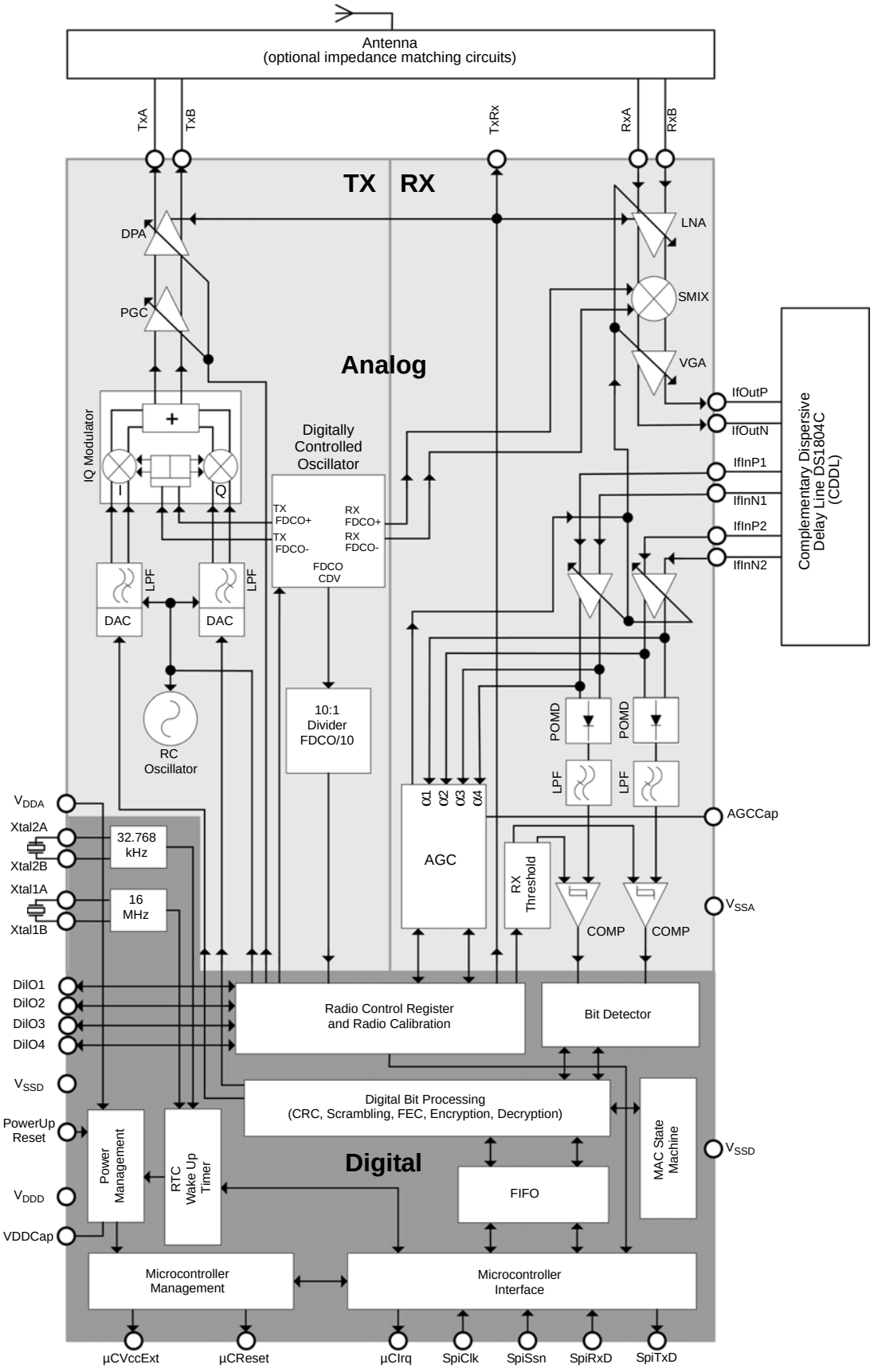

Figure 1: nanoNET TRX Transceiver block diagram (simplified)

5 Absolute Maximum Ratings

Table 2: Absolute maximum ratings

Parameter	Value	Units	Item
Maximum received power	-20	dBm	5.1
Temperatures			5.2
Operating temperature (operating ambient temperature range)	+85	°C	5.3
Operating junction temperature (operating junction temperature range in TX mode)	+95	°C	5.4
Operating junction temperature (operating junction temperature range in RX mode)	+90	°C	5.5
Storage temperature (storage temperature range)	+125	°C	5.6
Reflow solder temperature (lead-free package)	+242	°C	5.7
Total power dissipation	450	mW	5.8
Supply voltage (V_{DDA}, V_{DDD})	3.6	V	5.9

It is critical that the ratings provided in *Absolute Maximum Ratings* on page 6 be carefully observed. Stress exceeding one or more of these limiting values may cause permanent damage to the device.

6 Pin Connections (MLF44 7X7 mm)

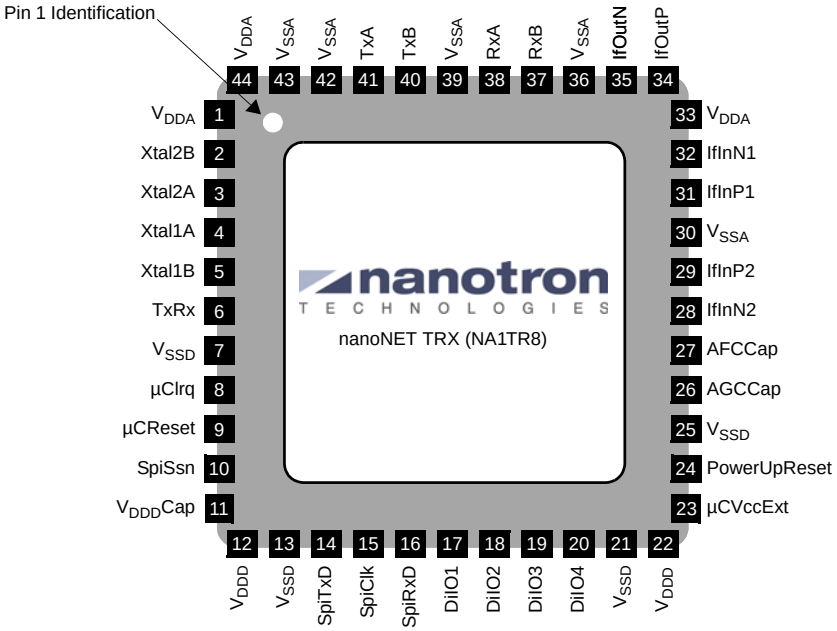

Figure 2: nanoNET TRX (MLF44) pin connections

Note: The pinning of the *nanoNET TRX Transceiver* described in this datasheet includes a 44 pin package. See *Package Dimensions* on page 30.

7 Pin Description

Table 3: nanoNET TRX Transceiver (NA1TR8) pin description

Pin	Name	Type	Description	Item
1	V_{DDA}	–	Power supply for analog part.	7.1
2	Xtal2B	Input	Input for 32.768 kHz quartz oscillator.	7.2
3	Xtal2A	Input	Input for 32.768 kHz quartz oscillator.	7.3
4	Xtal1A	Input	Input for 16 MHz reference quartz oscillator.	7.4
5	Xtal1B	Input	Input for 16 MHz reference quartz oscillator.	7.5
6	TxRx	Output	External power amplifier control pin. Allows the use of an external amplifier. When activated by the register RfTxExtPampEnOutEn, this pin goes to low during TX mode. During non-transmit cycles, it has high-impedance. When not activated, it always has high-impedance.	7.6
7	V_{SSD}	–	Ground (digital).	7.7
8	µCIrq	Output	Interrupt request to external microprocessor.	7.8
9	µCReset	Output	Reset for external microprocessor.	7.9
10	SpiSsn	Input	Serial Peripheral Interface Slave Select (low active) is externally asserted before the microcontroller (master) can exchange data with the *nanoNET TRX* IC. Must be low before data transactions and must stay low for the duration of the transaction.	7.10
11	V_{DDD}Cap	–	V_{DDD} blocking capacitor pad used for blocking the internal digital power supply by at least one 100nF capacitor connected to VSSD. See *Figure 14:Example application showing recommended circuitry* on page 23	7.11
12	V_{DDD}	–	Power supply for digital part.	7.12
13	V_{SSD}	–	Ground (digital).	7.13
14	SpiTxD	Output	Serial Peripheral Interface Transmit Data (MISO).	7.14
15	SpiClk	Input	Serial Peripheral Interface Clock is generated by the microcontroller (master) and synchronizes data movement in and out of the device through the SpiRxD and SpiTxD respectively.	7.15
16	SpiRxD	Input	Serial Peripheral Interface Receive Data (MOSI).	7.16
17	DiIO1	Input/ Output	Digital Input or Output (programmable), line 1.	7.17
18	DiIO2	Input/ Output	Digital Input or Output (programmable), line 2.	7.18
19	DiIO3	Input/ Output	Digital Input or Output (programmable), line 3.	7.19

Table 3: nanoNET TRX Transceiver (NA1TR8) pin description

Pin	Name	Type	Description	Item
20	DiIO4	Input/ Output	Digital Input or Output (programmable), line 4. **Note**: 32.768 kHz clock operating on this pin after reset/ power up.	7.20
21	V_{SSD}	–	Ground (digital).	7.21
22	V_{DDD}	–	Power supply for digital part.	7.22
23	µCVccExt	Output	Power supply for external microprocessor	7.23
24	Power UpReset	Input	Power up reset line.	7.24
25	V_{SSD}	Input	Ground (digital).	7.25
26	AGCCap	–	Capacitor for AGC.	7.26
27	AFCCap	–	Capacitor for AFC.	7.27
28	IfInN2	Input	IF Input (channel 2, down-chirp) - connected to port B of Complementary Dispersive Delay Line (CDDL), line N.	7.28
29	IfInP2	Input	IF Input (channel 2, down-chirp) - connected to port B of Complementary Dispersive Delay Line (CDDL), line P.	7.29
30	V_{SSA}	–	Ground (analog).	7.30
31	IfInP1	Input	IF Input (channel 1, up-chirp) - connected to port C of Complementary Dispersive Delay Line (CDDL), line P.	7.31
32	IfInN1	Input	IF Input (channel 1, up-chirp) - connected to port C of Complementary Dispersive Delay Line (CDDL), line N.	7.32
33	V_{DDA}	–	Power supply for analog part.	7.33
34	IfOutP	Output	IF Output - connected to port A of Complementary Dispersive Delay Line (CDDL), line P.	7.34
35	IfOutN	Output	IF Output - connected to port A of Complementary Dispersive Delay Line (CDDL), line N.	7.35
36	V_{SSA}	–	Ground (analog).	7.36
37	RxB	Input	Receiver input.	7.37
38	RxA	Input	Receiver input.	7.38
39	V_{SSA}	–	Ground (analog).	7.39
40	TxB	Output	Transmitter output.	7.40
41	TxA	Output	Transmitter output.	7.41
42	V_{SSA}	–	Ground (analog).	7.42

Table 3: nanoNET TRX Transceiver (NA1TR8) pin description

Pin	Name	Type	Description	Item
43	V_{SSA}	–	Ground (analog).	7.43
44	V_{DDA}	–	Power supply for analog part.	7.44

8 Electrical Specifications

8.1 General DC Parameters

Table 4: General DC parameters

Parameter	Min	Typical	Max	Unit	Item
Operating frequency range	2400	2441.750	2483.5	MHz	8.1.1
Supply voltage range $V_{DDA} \cong V_{DDD}$	2.4	3.0	3.6	V	8.1.2
Modulation method	–	Chirp	–	–	8.1.3
Operating temperature range	-40	+25	+85	°C	
Supply current[a]					8.1.4
Power down (Internal Real Time Clock Active)	–	1.5	4	µA	8.1.5
Power up	–	150	200	µA	8.1.6
Standby	–	2.4	2.6	mA	8.1.7
Ready	–	9.6	10.5	mA	8.1.8
RX (up/down)	–	35	–	mA	8.1.9
TX (P_{out} = *+8 dBm*)	–	82	–	mA	8.1.10
Supply Voltage					8.1.11
V_{DDA} supply voltage	2.4	3	3.6	V	8.1.12
V_{DDD} supply voltage	2.4	3	3.6	V	8.1.13
V_{IL} (low level input voltage)[b]	-0.3	–	0.8	V	8.1.14
V_{IH} (high level input voltage)[b]	2.0	–	V_{DDD} + 0.3	V	8.1.15
V_{OL} (low level output voltage)	–	–	0.4	V	8.1.16
V_{OH} (high level output voltage)	2.4	–	–	V	8.1.17
I_{OH} (high output current)	-2	–	–	mA	8.1.18
I_{OL} (low output current)	2	–	–	mA	8.1.19

a. Under nominal conditions, except otherwise specified.
b. Given only for V_{dd} = 3.0 to 3.6

8.2 Transmitter (TX) Parameters

Under nominal conditions unless specified. See *Nominal Conditions* on page 2.

Table 5: Transmitter (TX) parameters

Parameter	Min	Typical	Max	Unit	Item
Transmitter nominal output power[a]	6	8	–	dBm	8.2.1
Transmitter output power controlled in steps	–	Yes	–		8.2.2
Dynamic for output power control	–	39	–	dB	8.2.3
Number of steps for output power control	–	19	–	–	8.2.4
Load impedance	–	150	–	Ω	8.2.5
Type of load	–	Balanced	–		8.2.6
Transmitter spurious emissions[b] (1 GHz ... 12.5 GHz)	–	–	-80	dBm/Hz	8.2.7
Transmitter carrier suppression	–	-20	–	dBc	8.2.8
Carrier frequency	–	2441.750	–	MHz	8.2.9
Carrier frequency accuracy	-0.5	± 0.275	+0.5	MHz	8.2.10
Chirp sample frequency	–	244.175	–	MHz	8.2.11
Reference quartz oscillator					8.2.12
Quartz operating frequency	–	16	–	MHz	8.2.13
Recommended accuracy	–	± 50	–	ppm	8.2.14
Maximum equivalent serial resistance of the quartz resonator	–	–	50	Ω	8.2.15
Load capacitance of quartz resonator	–	27	–	pF	8.2.16

a. The transmitter output power is the average power related to the peak envelope power of the chirp waveform. (Due to shape of the waveform envelope, the measured average power of the chirp is about 1dB smaller than the peak envelope power.)

b. The maximum transmitter output power has to be adjusted to ≤8 dBm to secure from overdrive.

8.3 Receiver (RX) Parameters

Under nominal conditions unless specified. See *Nominal Conditions* on page 2.

Note: The measurement results provided in this table were reached by using CDDL. For information on the CDDL, refer to the *Complementary Dispersive Delay Line Datasheet.*

Table 6: Receiver (RX) parameters

Parameter	Min	Typ	Max	Unit	Item
Receiver sensitivity @ 1 Mbps	–	-92	–	dBm	8.3.1
Receiver sensitivity @ 2 Mbps	–	-86	–	dBm	8.3.1
Input impedance @ 2.44 GHz[a]	–	7–j56	–	Ω	8.3.2
Type of input	–	Balanced	–	–	8.3.3
Center frequency	–	2441.75	–	MHz	8.3.4
Gain from receiver input up to input to dispersive delay line (CDDL)[a]	–	64	–	dB	8.3.5
LO frequency	–	2691.75	–	MHz	8.3.6
LO frequency accuracy	-0.5	± 0.275	0.5	MHz	8.3.7
LO rejection noise $P_{RX\text{-}LO}$ @ *LNA* input pin	–	–	-40	dBm	8.3.8
Programmable frequency step[b]	–	± 500	–	kHz	8.3.9
IF frequency (center)	–	250	–	MHz	8.3.10
IF frequency bandwidth (*-3 dB*)[a] (determined by CDDL)	90	–	–	MHz	8.3.11
IF output impedance (balanced) @ 250 MHz[a]	–	100	–	Ω	8.3.12
Type of IF output	–	Balanced	–	–	8.3.13
Impedance of IF input 1 (balanced) @ 250 MHz[a]	–	1.6	–	kΩ	8.3.14
Impedance of IF input 2 (balanced) @ 250 MHz[a]	–	1.6	–	kΩ	8.3.15
Type of IF1, IF2 input	–	Balanced	–	–	8.3.16
Maximum received power	–	–	-20	dBm	8.3.17

a. Simulated results.
b. The minimum change frequency of the LO.

8.4 Digital Interface Parameters

Under nominal conditions unless specified. See *Nominal Conditions* on page 2.

Table 7: Digital sensor/actuator interface parameters

Parameter	Value	Unit	Item
Number of independent digital interfaces[a]	4	Number	8.4.1
Width of each interface	1	bit	8.4.2
Direction	Programmable	–	8.4.3
Type	In/Out (bi-directional, open-drain with pull-up)	–	8.4.4

a. At Pin number 4 (DilO4), 32.768 kHz clock operating after reset/power up.

8.5 Power Management and Sleep/Wake-Up Circuitry Parameters

Under nominal conditions unless specified. See *Nominal Conditions* on page 2.

Table 8: Power management and sleep/wake-up circuitry parameters

Description	Min	Typical	Max	Unit	Item
Real Time Clock (RTC)					8.5.1
Quartz operating frequency	–	32.768	–	kHz	8.5.2
Recommended accuracy	–	± 50	–	ppm	8.5.3
Load capacitance of quartz resonator	–	12.50	–	pF	8.5.4
Maximum equivalent serial resistance of quartz resonator	–	–	50	kΩ	8.5.5
RTC register length	–	48	–	bit	8.5.6
Epoch date	–	01.01.1970	–	Date	8.5.7
Battery monitor					8.5.8
Battery monitor voltage	2.4	2.7	3.6	V	8.5.9
Basic dynamic performance (Note: Values in this section are simulation results only)					8.5.10
Switch time from TX to RX (from Ack to Data mode)	–	24	–	µs	8.5.11

Table 8: Power management and sleep/wake-up circuitry parameters

Description	Min	Typical	Max	Unit	Item
Switch time from TX to RX (from Data to Ack mode)	–	8	–	µs	8.5.12
Switch time from RX to TX (from Ack to Data mode)	–	24	–	µs	8.5.13
Switch time from RX to TX (from Data to Ack mode)	–	8	–	µs	8.5.14
Turn-on time TX (user command received via SPI and begin of packet transmission)	–	24	–	µs	8.5.15
Turn-on time RX (user command received via SPI and begin of packet reception)	–	6	–	µs	8.5.16
Startup Time for *16 MHz* XTAL until stable frequency generation	1.5	–	5	ms	8.5.17
Calibration time	–	≈2	–	ms	8.5.18

8.6 Interface to Digital Controller Parameters

Under nominal conditions unless specified. See *Nominal Conditions* on page 2.

Table 9: Interface to digital controller parameters

Symbol	Description	Min	Typical	Max	Unit	Notes	Item
µCVccExt	High current output / high impendance Voltage @ 10mA load	VDD - 100	VDD - 20	VDD	mV	Maximum current output = 10mA / high imped-ance mode	8.6.1
µCReset	Push-pull, tristate	–	–	–	V	See footnote[a]	8.6.2
µCIRQ	Push-pull	–	–	–	V	See footnote[a] .	8.6.3
SpiRxD SpiClk, SpiSSn	Input	–	–	–	V	See footnote[a]	8.6.4
SpiTxD	Open-drain or push-pull	–	–	–	V	See footnote[a]	8.6.5

a. V_{cc} = 2.4V : V_{OH} = 2.0V, V_{IH} = 1.7V, V_{OL} = 0.2V, V_{IL} = 0.7V,
V_{cc} = 3.0..3.6V : V_{OH} = 2.4V, V_{IH} = 1.7..2.0V, V_{OL} = 0.2V, V_{IL} = 0.8V

Note: Level translator is required for 5V logic level microcontroller.

9 Timing Diagrams

Time values in the following diagrams are based on the values as shown in *Table 8: Power management and sleep/wake-up circuitry parameters* on page 14.

9.1 Switch Time from TX to RX (from Ack to Data mode)

The switch time from TX to RX (from Ack to Data mode), $t_{TxRxAckData}$, is 24 µs. (See item 8.5.11.)

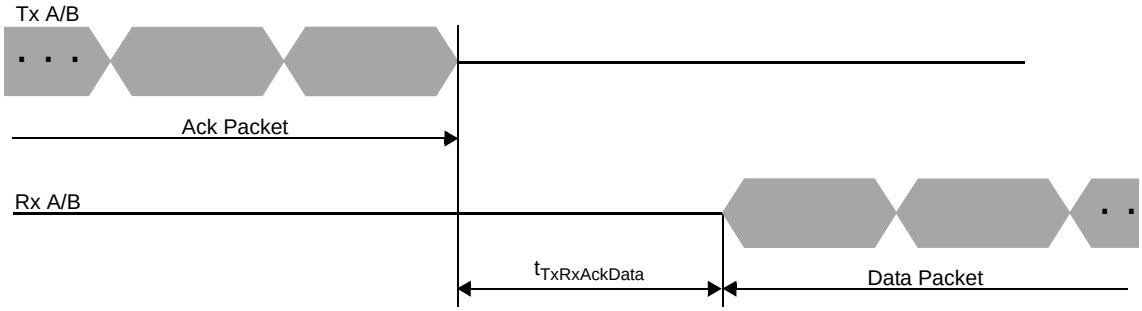

Figure 3: Switch time from TX to RX (from Ack to Data mode)

9.2 Switch Time from TX to RX (from Data to Ack mode)

The switch time from TX to RX (from Data to Ack mode), $t_{TxRxDataAck}$, is 8 µs. (See item 8.5.12.)

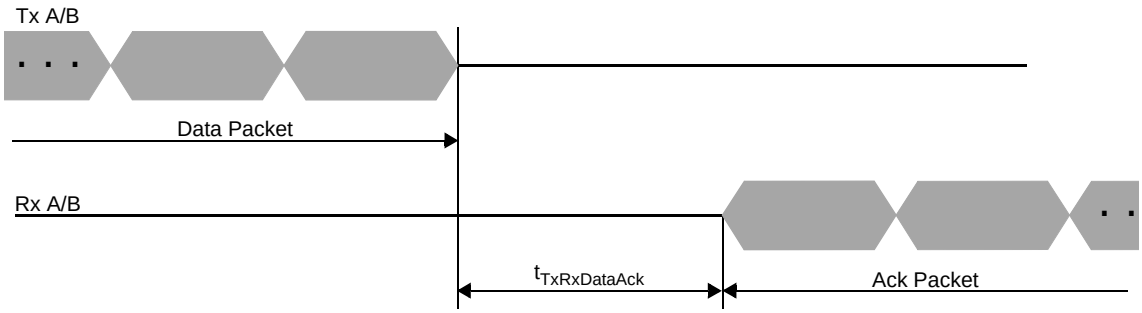

Figure 4: Switch time from TX to RX (from Data to Ack mode)

9.3 Switch Time from RX to TX (from Ack to Data mode)

The switch time from RX to TX (from Ack to Data mode), $t_{RxTxAckData}$, is 24 µs. (See item 8.5.13.)

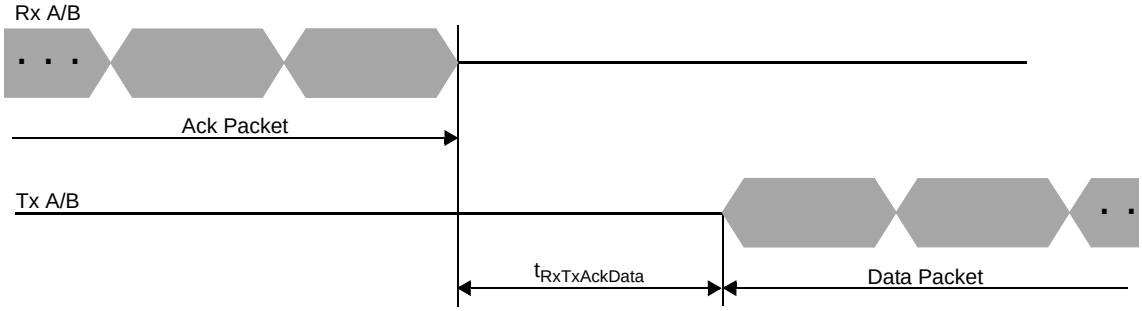

Figure 5: Switch time from RX to TX (from Ack to Data mode)

9.4 Switch Time from RX to TX (from Data to Ack mode)

The switch time from RX to TX (from Data to Ack mode), $t_{RxTxDataAck}$, is 8 µs. (See item 8.5.14.)

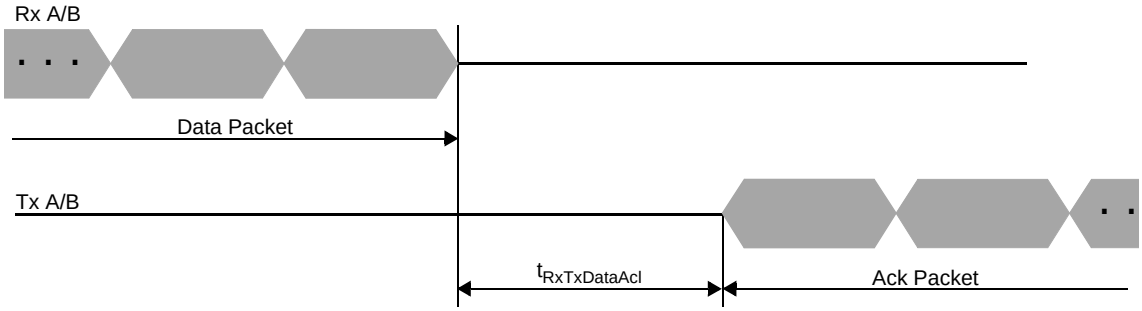

Figure 6: Switch time from RX to TX (from Data to Ack mode)

9.5 Turn-On Time TX

The Turn-on time for TX, t_{TxTO}, from the reception via SPI of a user command to the beginning of packet transmission is 24 µs. (See item 8.5.15.)

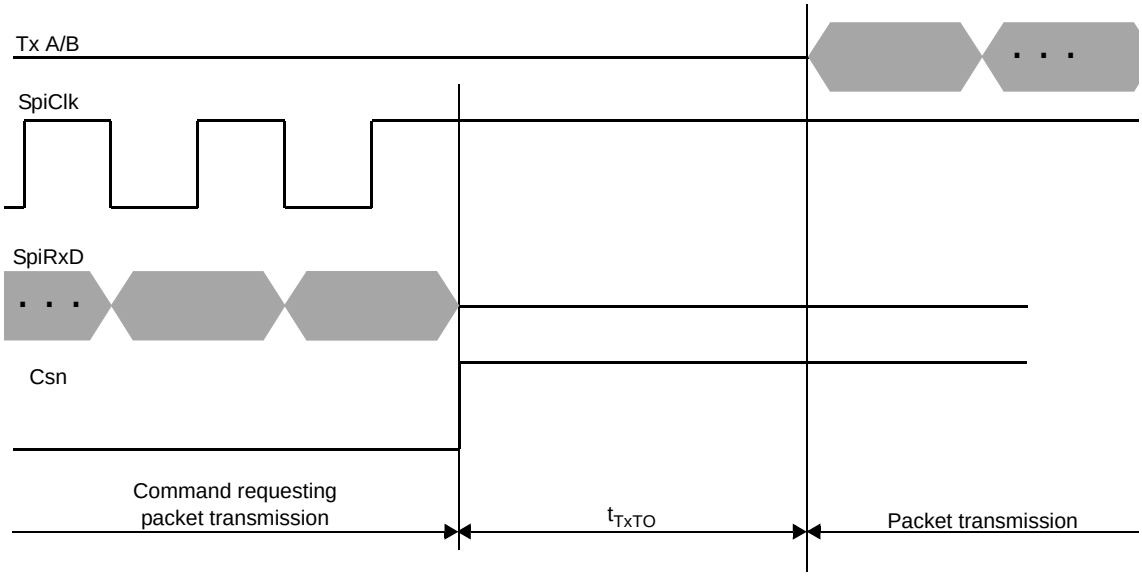

Figure 7: Turn-on time TX: time = t_{TxTO}

9.6 Turn-On Time RX

The Turn-on time for RX, t_{RxTO}, from the reception via SPI of a user command to the beginning of packet reception is 6 µs. (See item 8.5.16.)

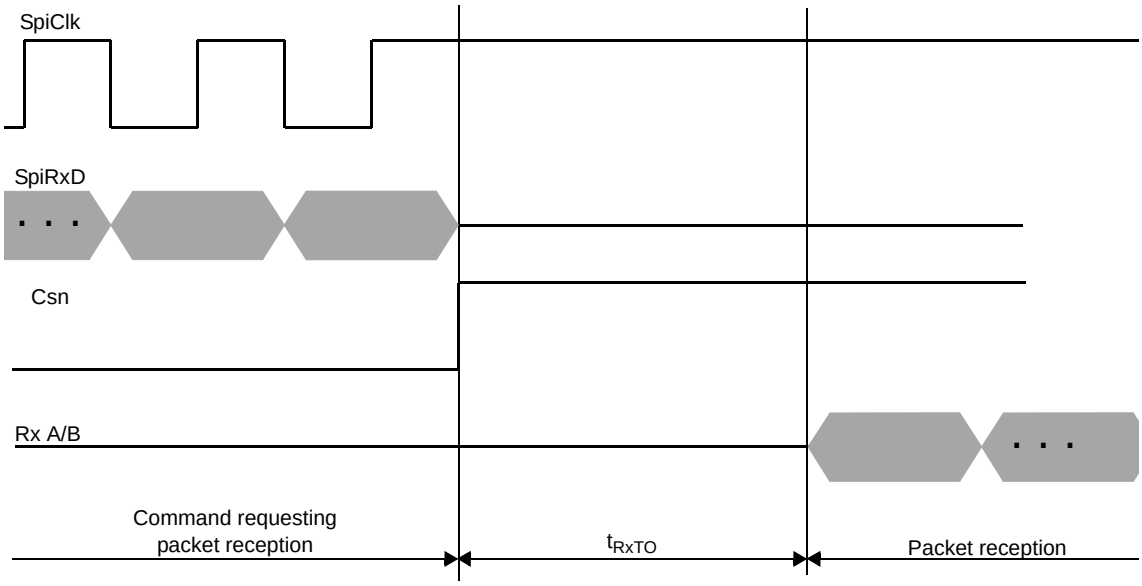

Figure 8: Turn-on time RX: time = t_{RxTO}

9.7 16 MHz Crystal Start-Up Time

The start-up time for the quartz oscillator until it reaches a stable frequency generation is within a range of 1.5 to 5 ms. See item 8.5.17 in *Table 8: Power management and sleep/wake-up circuitry parameters* on page 14.

9.8 LO Frequency Calibration Time

The time for the Local Oscillator frequency calibration, is approximately 2 ms. See item 8.5.18 in *Table 8: Power management and sleep/wake-up circuitry parameters* on page 14.

9.9 SPI Bus Read and Write Timing

The following timing diagrams shows the read and write timing of the SPI bus. For more details, see *nanoNET TRX Serial Peripheral Interface Specifications*.

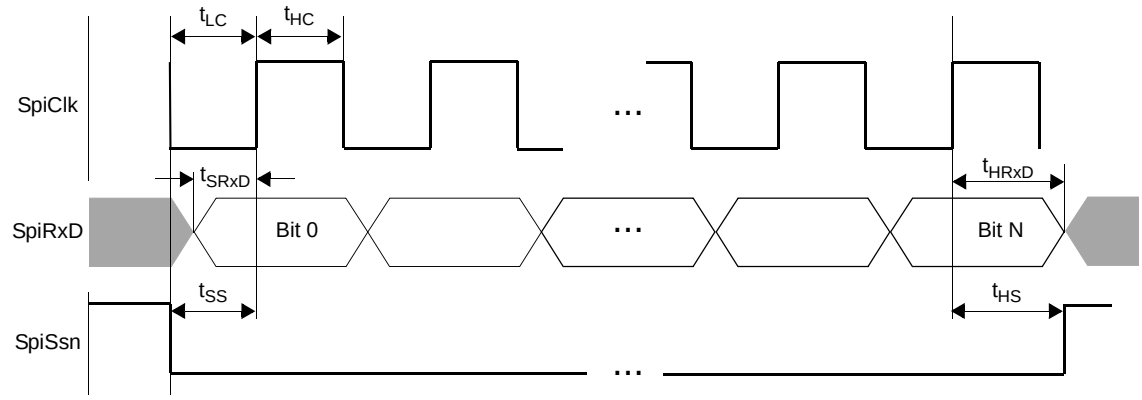

Figure 9: SPI bus write timing

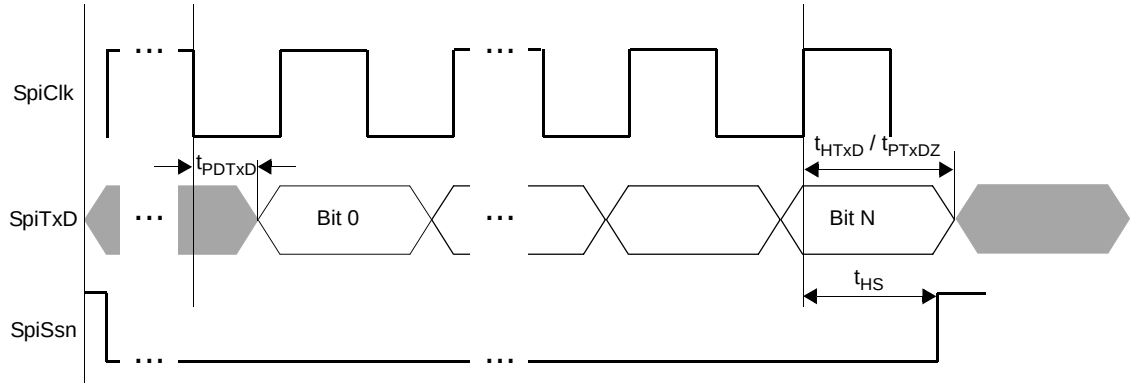

Figure 10: SPI bus read timing

The following table shows the SPI timing values.

Table 9: SPI timing values

Parameter	Min	Max	Comment
f_{max}	–	16 MHz	SpiClk
t_{LC}	22 ns	–	Low time SpiClk
t_{HC}	22 ns	–	High time SpiClk
t_{SS}	10 ns	–	SpiSsn Setup
t_{HS}	5 ns	-	SpiSsn Hold
t_{SRxD}	10 ns	–	SpiRxD Setup
t_{HRxD}	5 ns	–	SpiRxD Hold
t_{PDTxD}	–	18 ns	SpiTxD Propagation Delay Drive
t_{HTxD}	2 ns	–	SpiTxD Hold
t_{PTxDZ}	-	18 ns	SpiTxD Propagation Delay High Impedance

10 Output Power Control

The output power of the *nanoNET TRX Transceiver* can be set typically in a range of between -27 dBm to + 8 dBm. The following graphs show the range of possibilities. Nominal conditions except power supply voltage and RF output power.

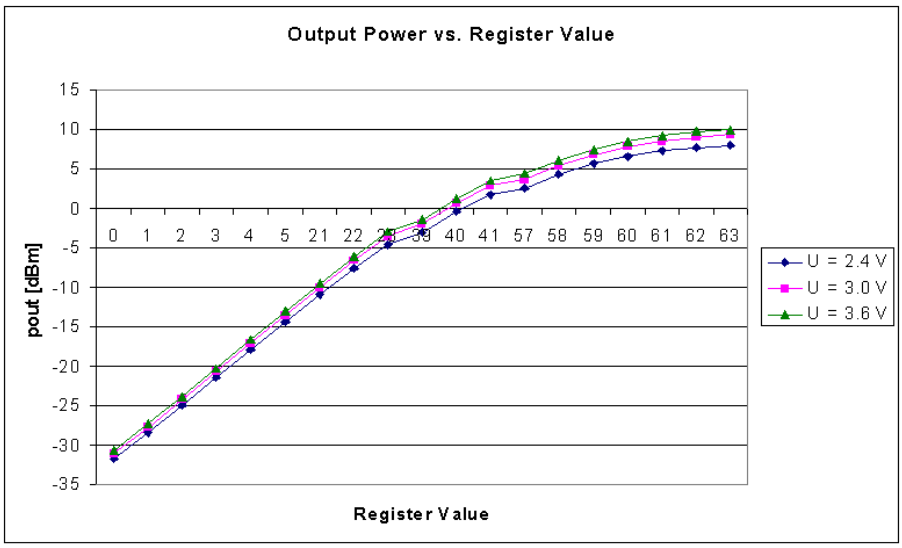

Figure 11: nanoNET TRX output power (pout[dBm] by register value)

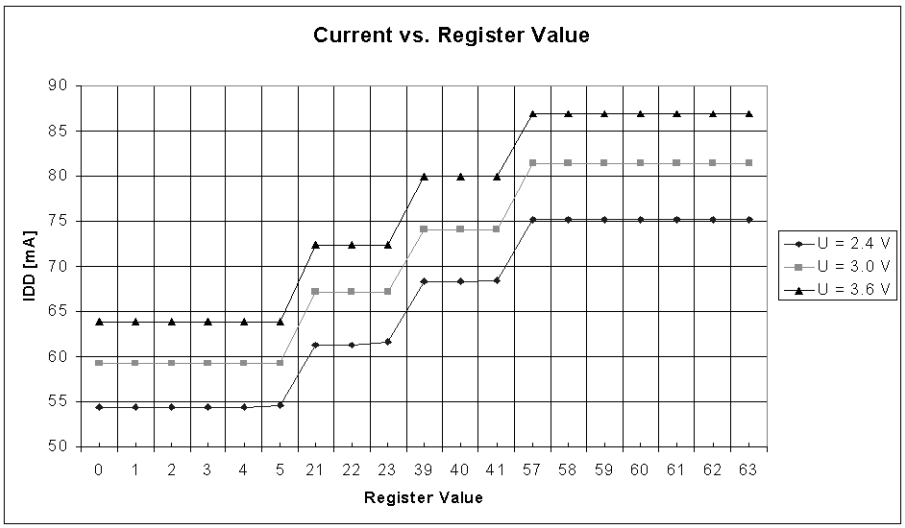

Figure 12: Total current consumption (IDDA[mA] by register value)

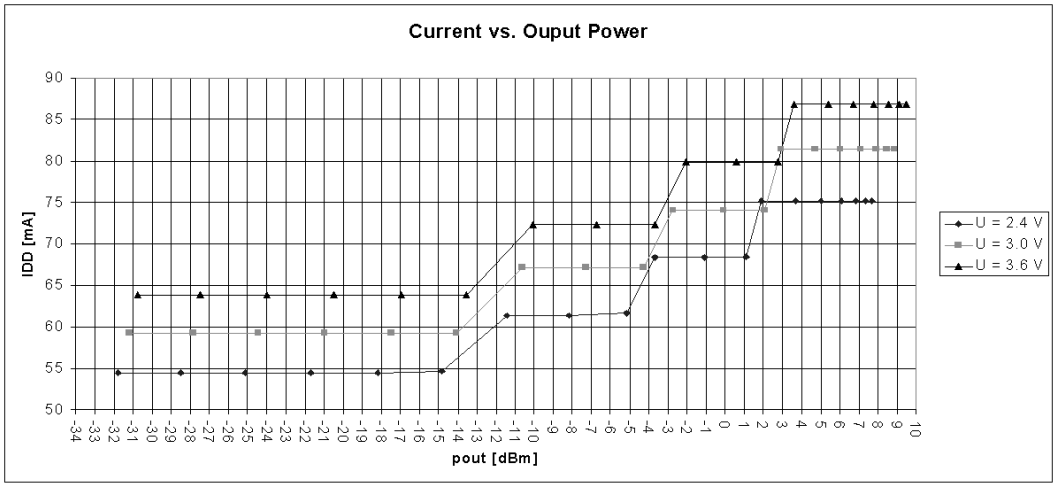

Figure 13: Total current consumption (IDDA[mA] by output power [dBm])

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11 Example Application

The following application is an example of the *nanoNET TRX Transceiver* used with a temperature measurement and control device.

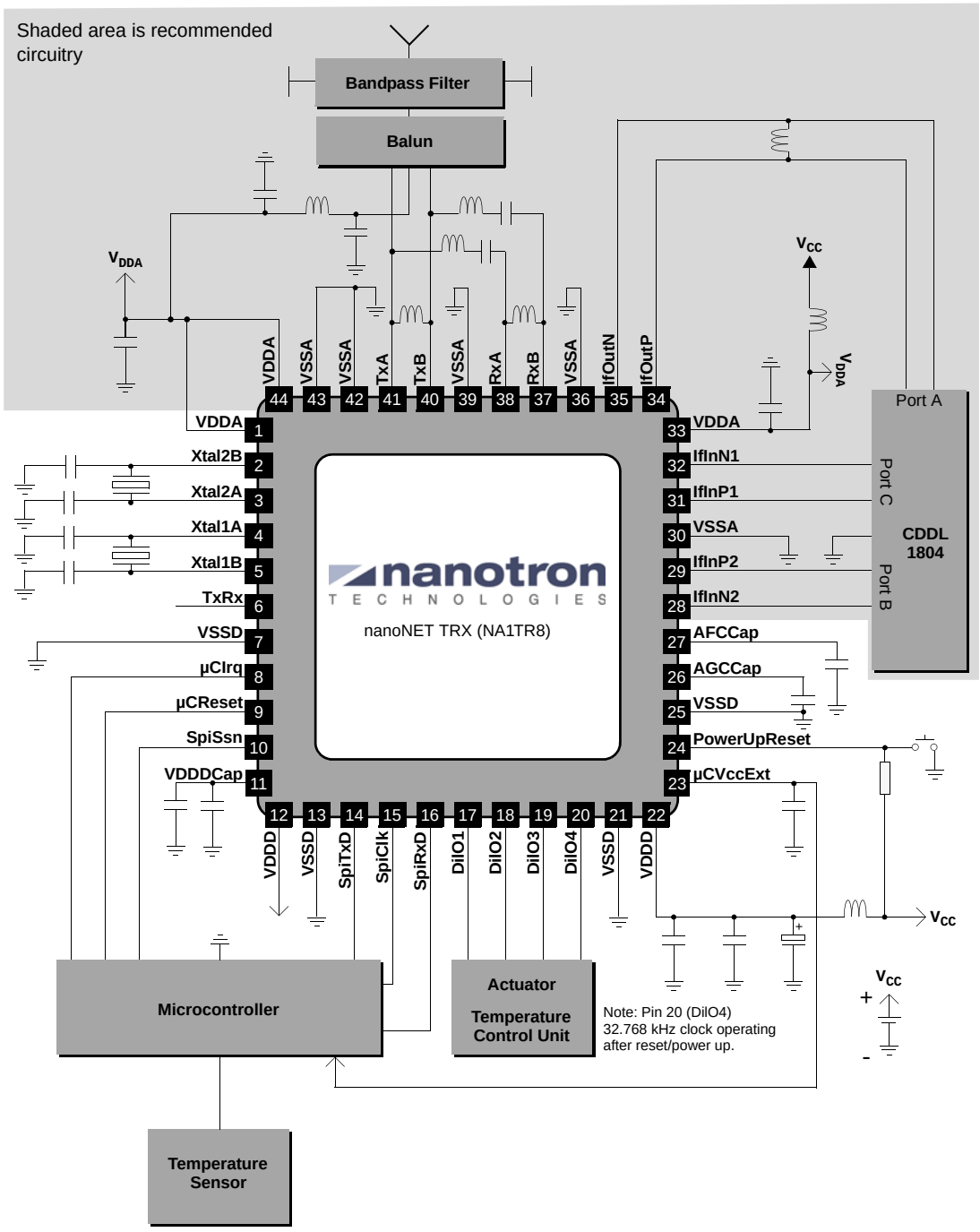


Figure 14: Example application showing recommended circuitry

12 Recommended PCB Layout for RF Part

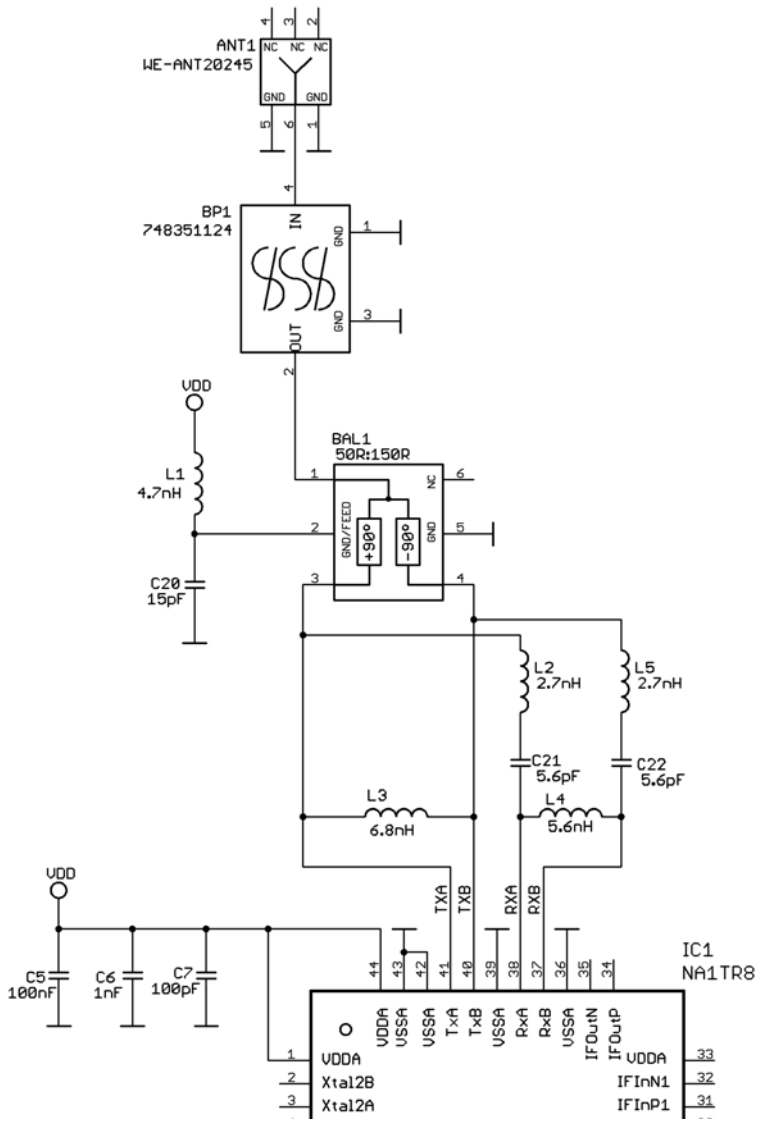


Figure 15: Recommended PCB layout for RF part: schematic 1 of 1

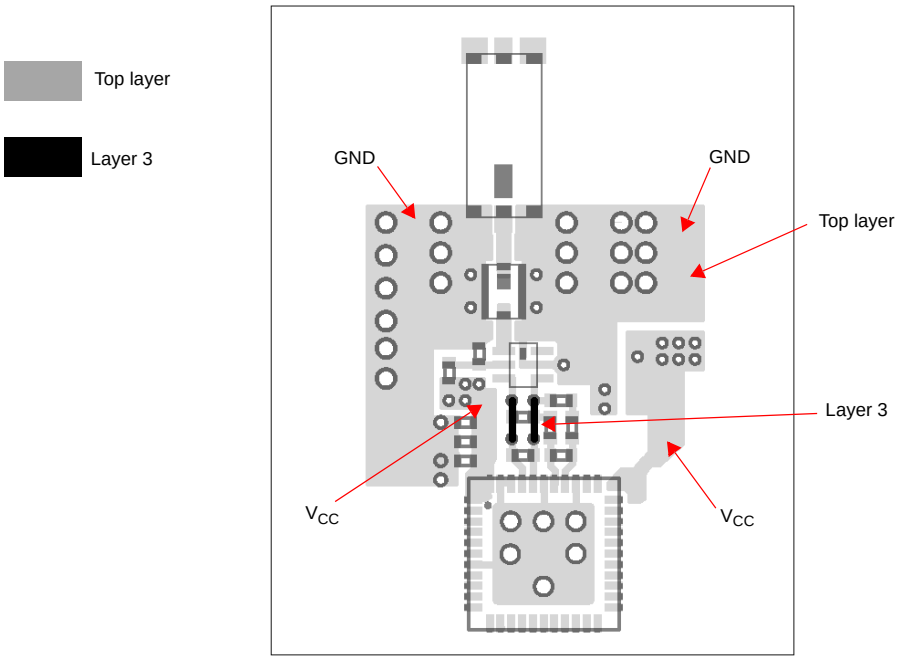


Figure 16: RF part: PCB board overview

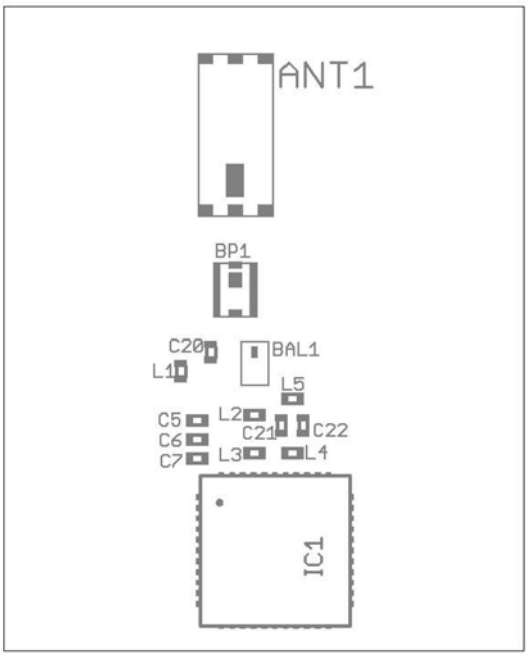


Figure 17: RF part: names

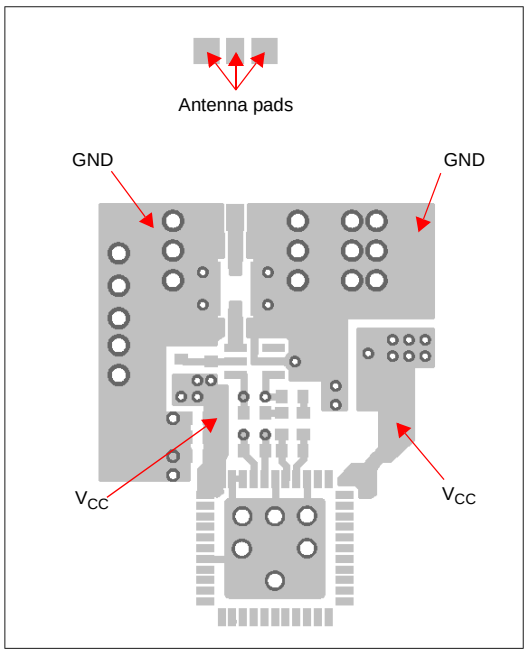


Figure 18: RF part: top layer

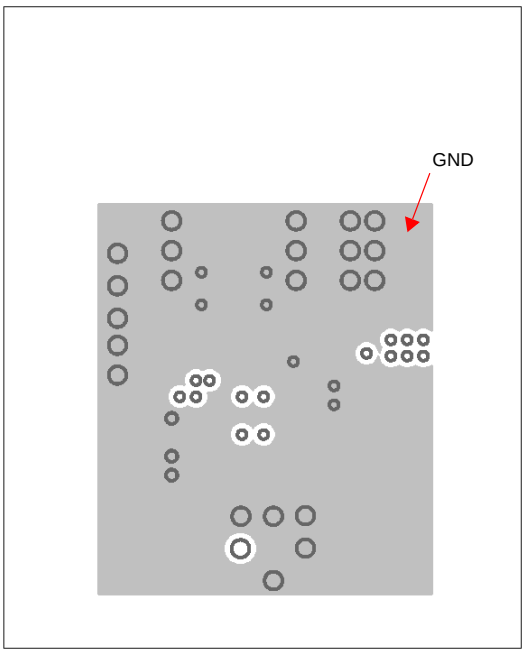


Figure 19: RF part: layer 2

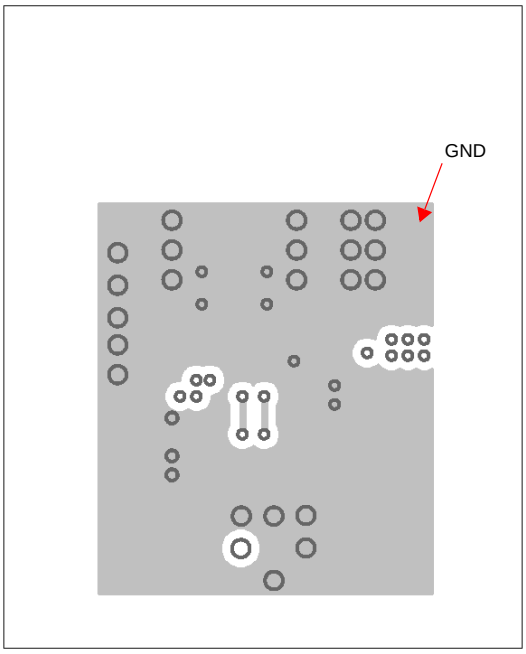


Figure 20: RF part: layer 3

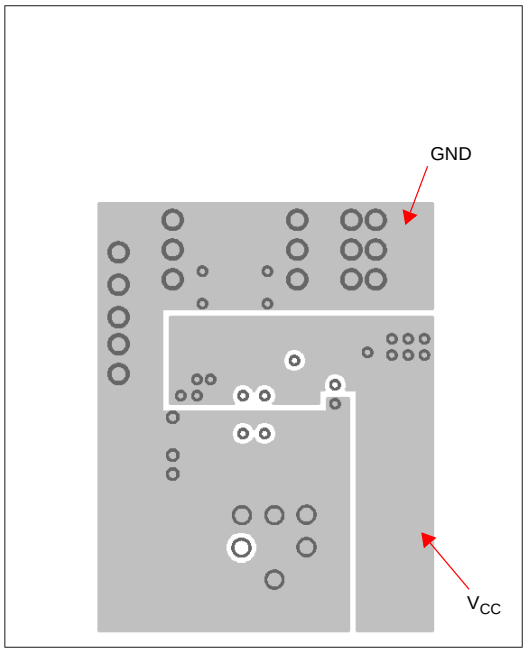


Figure 21: RF part: bottom layer

13 Recommended PCB Layout for IF Part

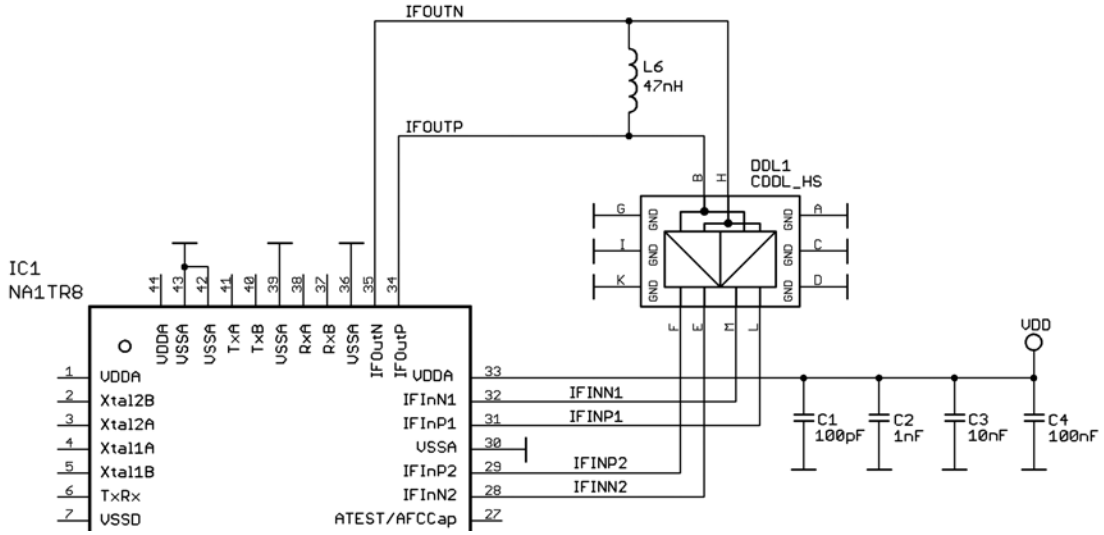


Figure 22: Recommended PCB layout for IF part: schematic 1 of 1

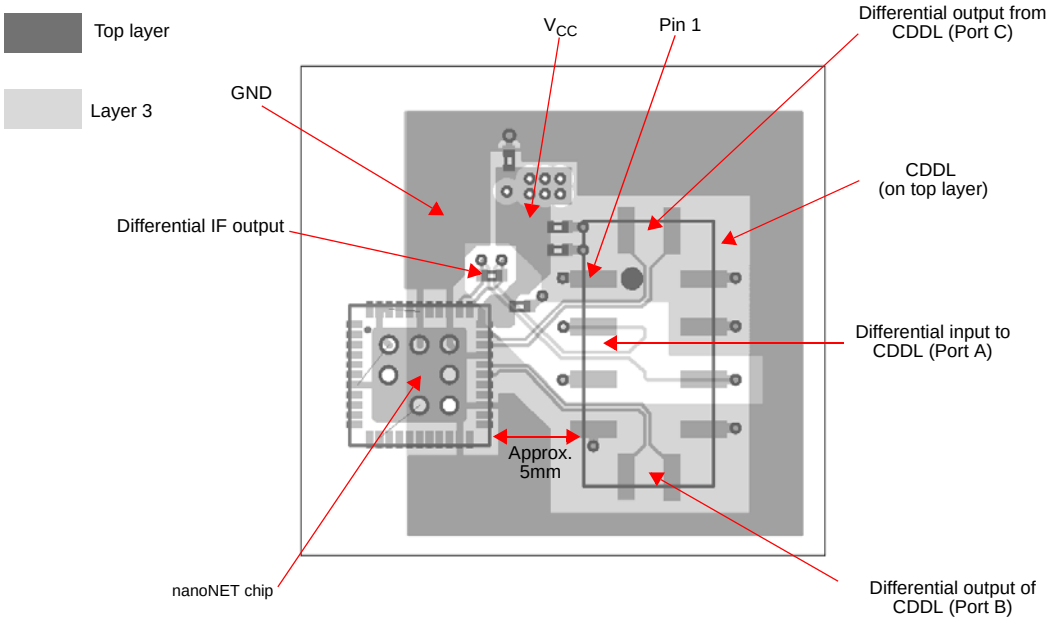


Figure 23: IF part: board overview

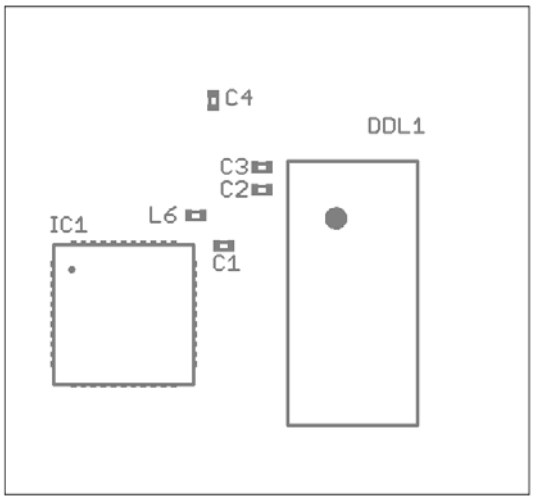


Figure 24: IF part: names

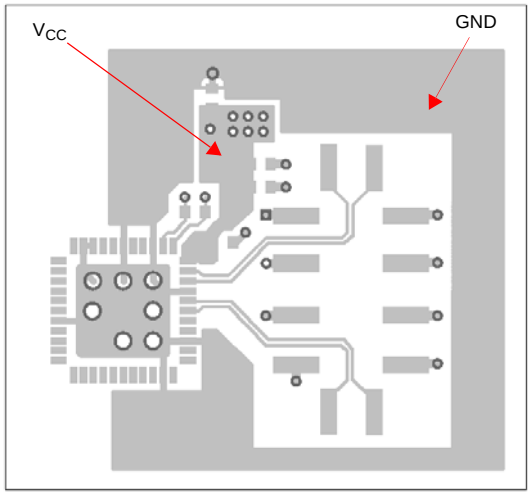


Figure 25: IF part: top layer

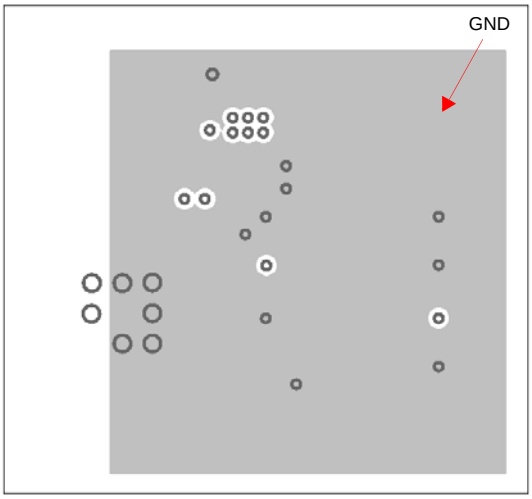


Figure 26: IF part: layer 2

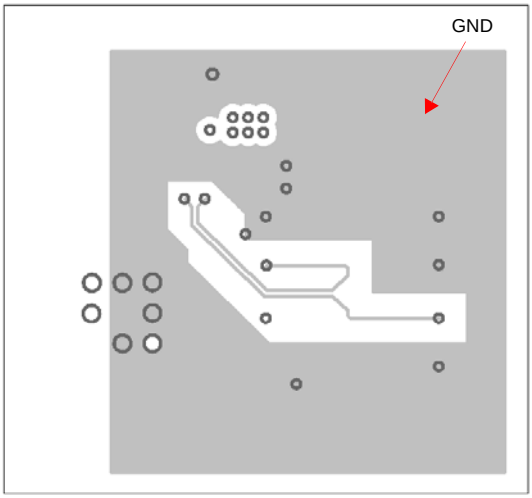


Figure 27: IF part: layer 3

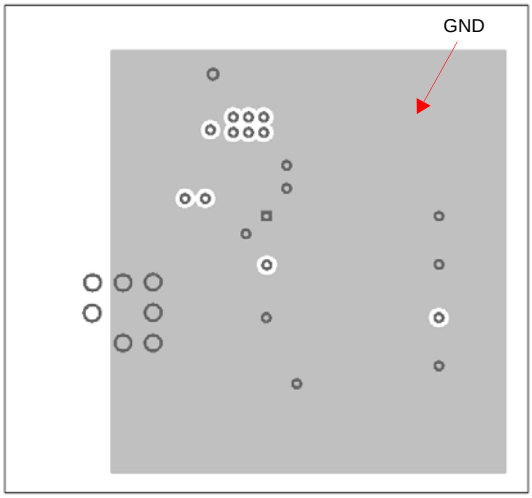


Figure 28: IF part: bottom layer

Recommended IF Layout Requirements

The following describes the layout requirements for the IF part:

- V_{SSA} pin is connected to the ground plan under the chip.
- Short connection between chip and CDDL, with minimal width of wires and minimal pad areas for minimal influence of PCB parasitics (do not implement 50 Ω microstrip).
- Equal lengths of traces for better CMRR.
- External coil (L1 = 47 nH) placed directly between the input pads of CDDL (PORT A).
- Use 4 layer PCB (top layer = layer 1, GND = inner layer 2, GND = inner layer 3, and bottom layer = layer 4).

14 Package Dimensions

The following shows the dimensions of MLF44 44 Pin 7x7 lead-free package.

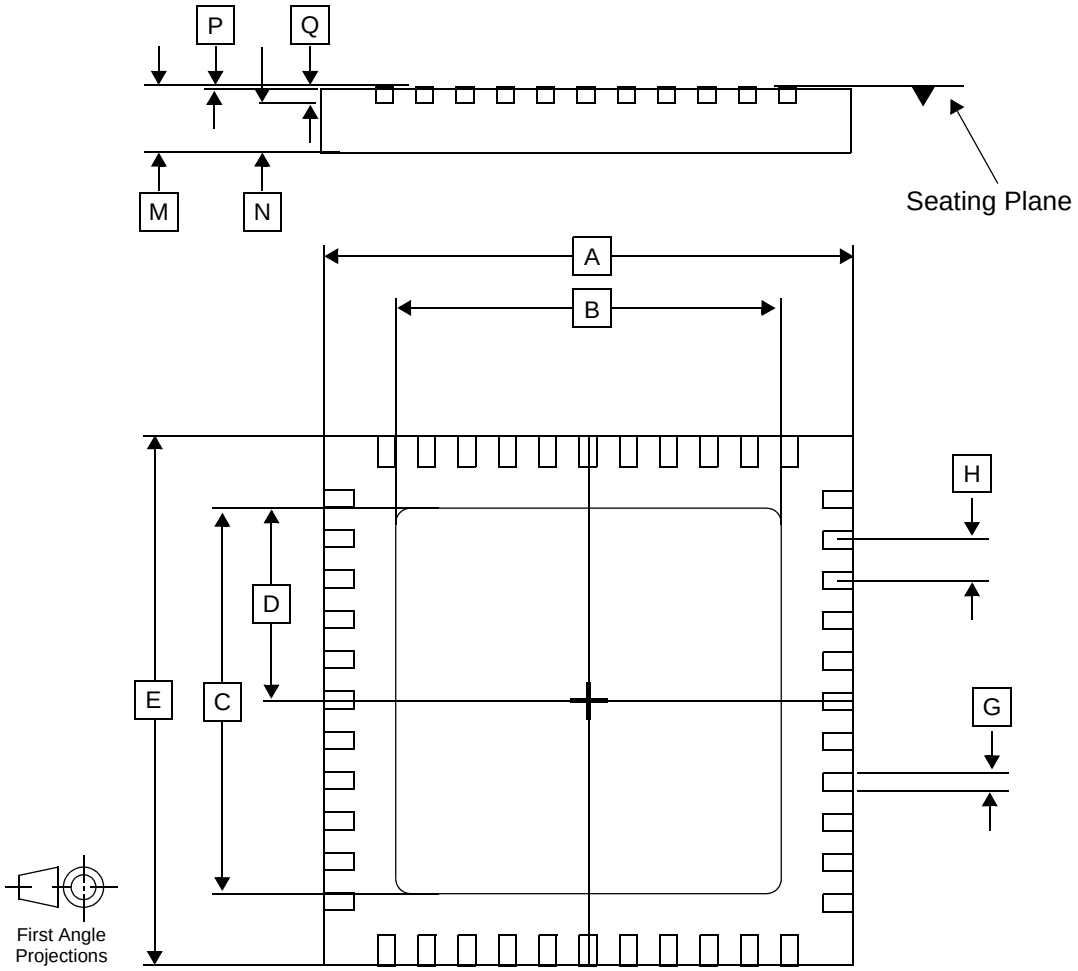


Figure 29: MLF44 7x7 package dimensions

Table 10: Package dimensions labels (unless specified, dimensions are in millimeters)

Label	Common Dimensions		
	Minimum	Nominal	Maximum
A		7.00	
B	4.55	4.70	4.85
C	4.55	4.70	4.85
D		C / 2	
E		7.00	
G	0.18	0.23	0.30
H		0.50	
M	0.80	0.9	1.00
N	–	0.65	0.80
P	0.00	0.02	0.05
Q		0.25	

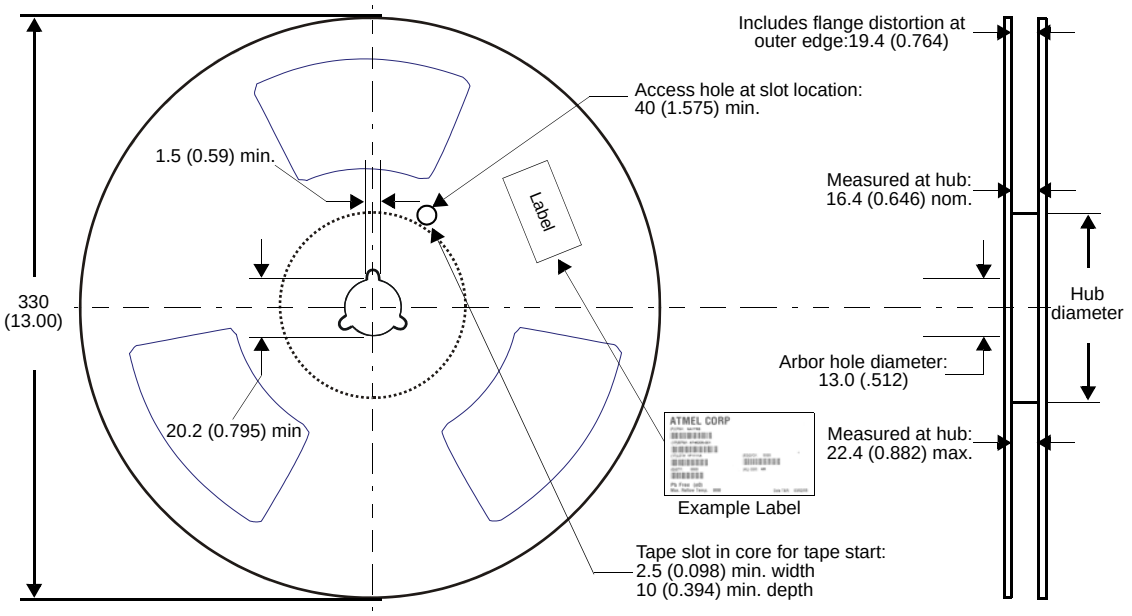
15 Tape and Reel Information

An embossed tape and reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for the *nanoNET TRX Transceiver (NA1TR8)* and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the peel-back cover tape.

15.1 Reel Dimensions

Reel Diameter	Units Per Reel	Reel and Hub Size[1]
13”	2,500	13/4

1. *Reel and hub size = 13 inch reel with 4 inch hub.*



Note: Dimensions are in millimeters (inches are in brackets for reference purposes only).

Figure 30: Reel dimensions

15.2 Tape Dimensions

Package Type	Number of Leads	Nominal Package Size	Carrier Tape Width	Carrier Tape Pitch	Leader/Trailer Length[1]
QFN (MLFP)	44	7 x 7 x 0.9 mm	16 mm	12 mm	EIA

1. *The device loading orientation is in compliance with EIA-481.*

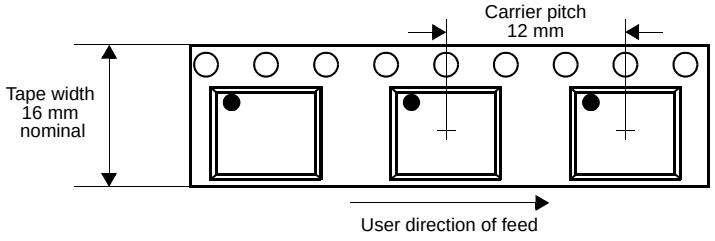


Figure 31: Tape dimensions

16 Ordering Information

To order the product described in this datasheet, use the following information.

Part Number	Package Type	Package Quantity	RoHS Compliant[1]
NA0108B	MLF 44 7x7 mm Tape and reel	16 x 12 type 2,500 pieces per tape	Yes. A certificate of RoHS compliance is available from Nanotron Technologies on request.

1. The RoHS directive is “The Restriction of Hazardous Substances in Electrical and Electronic Equipment (ROHS) Directive (2002/95/EC)”. The Directive aims to protect human health and the environment by restricting the use of certain hazardous substances in new equipment; and it complements the WEEE Directive.

A1 Reference Design

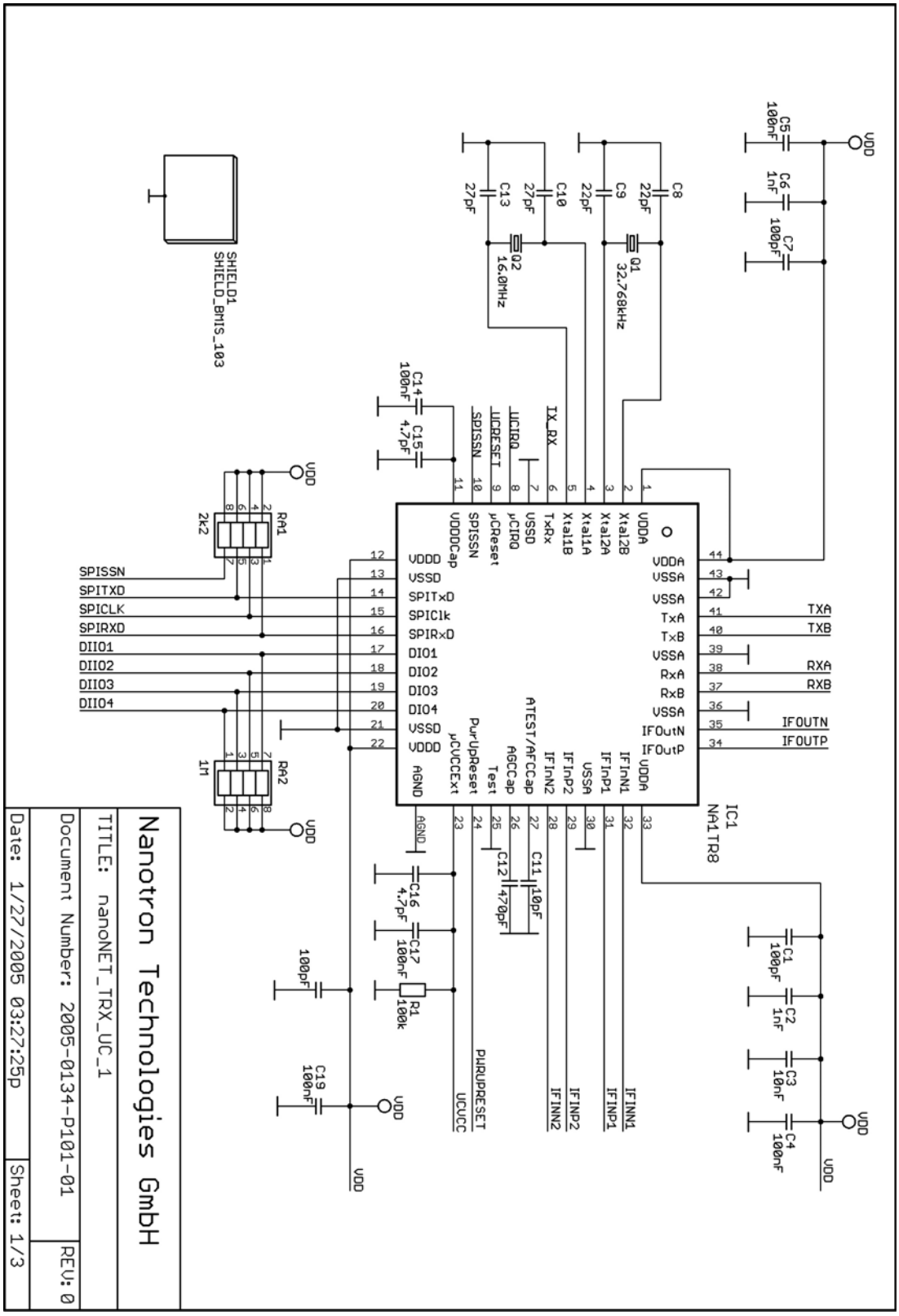


Figure 32: Reference design: schematic 1 of 3

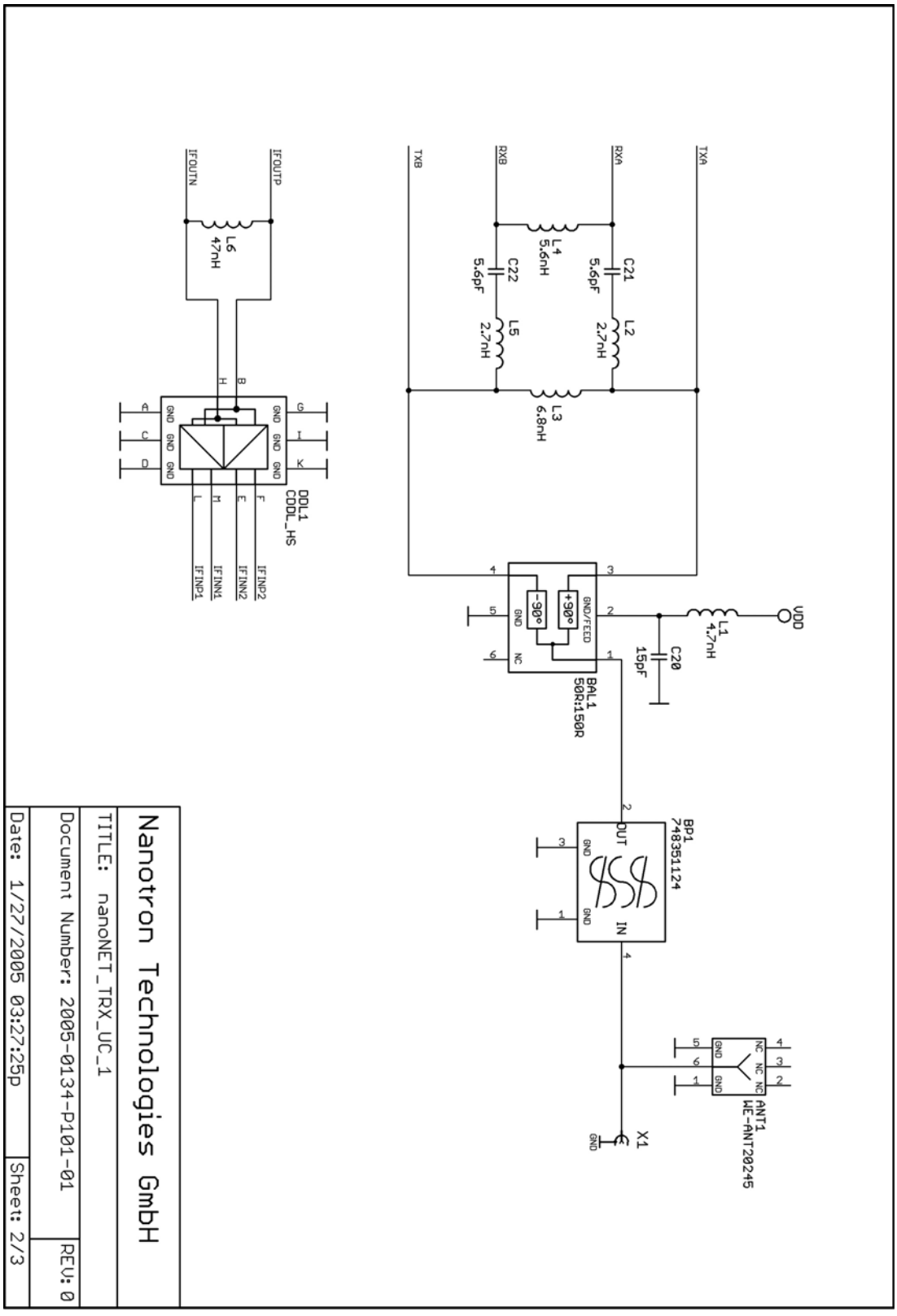


Figure 33: Reference design: schematic 2 of 3

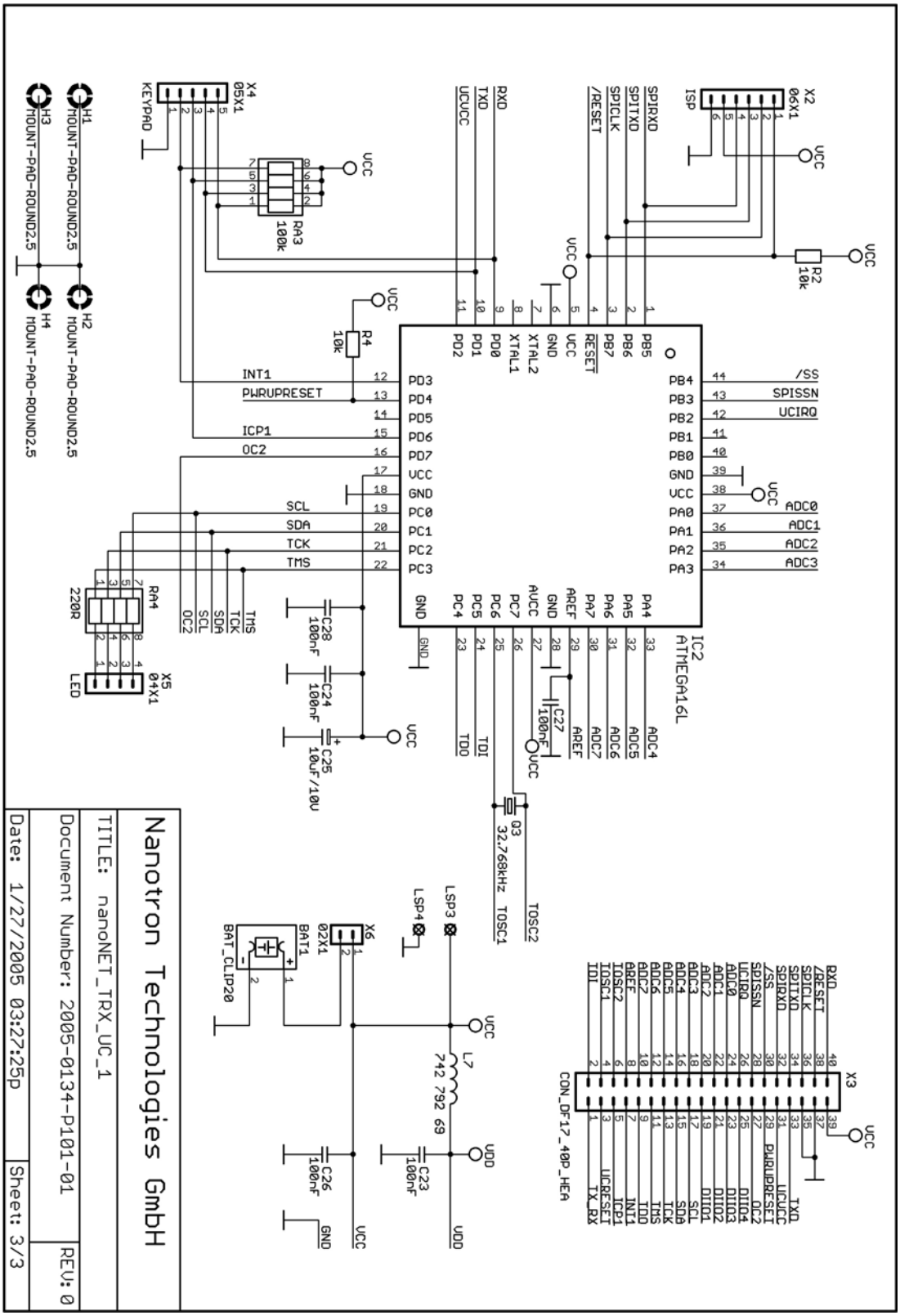


Figure 34: Reference design: schematic 3 of 3

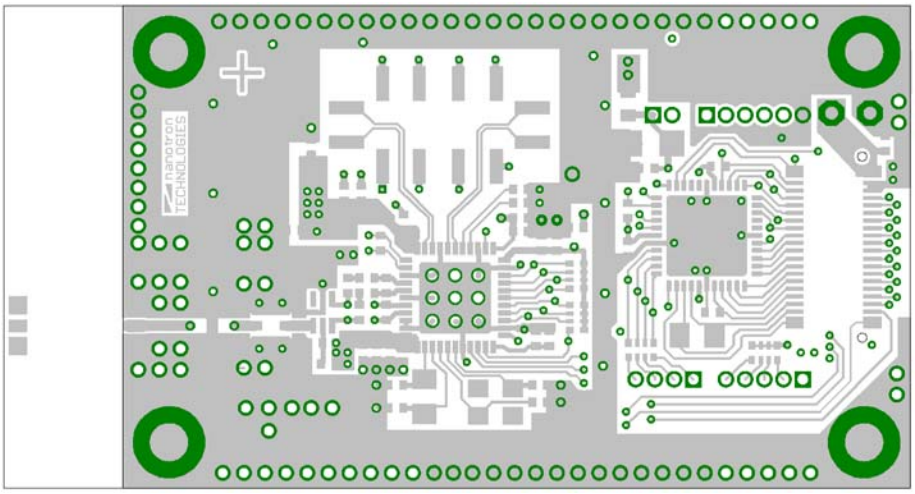


Figure 35: Reference design: top layer

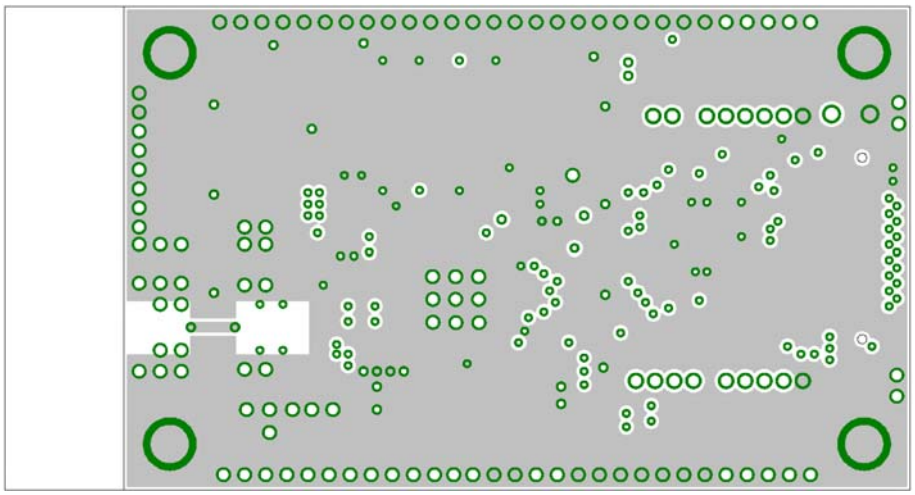


Figure 36: Reference design: layer 2

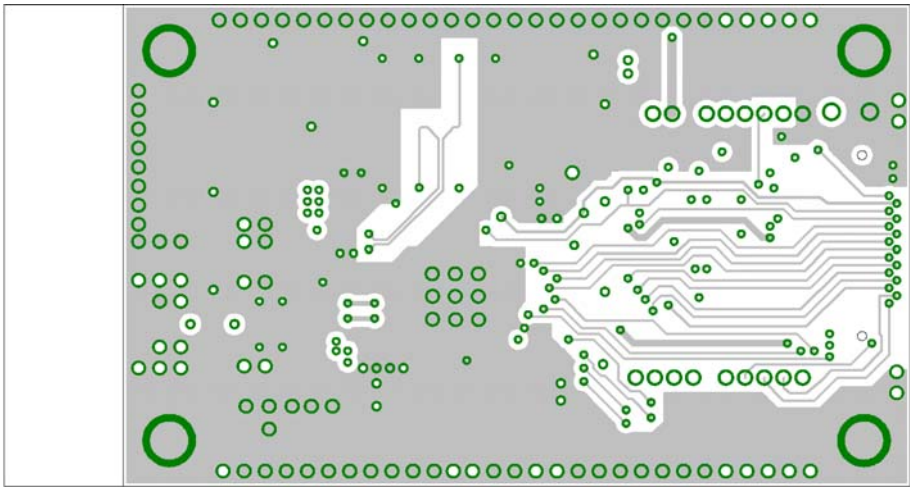


Figure 37: Reference design: layer 3

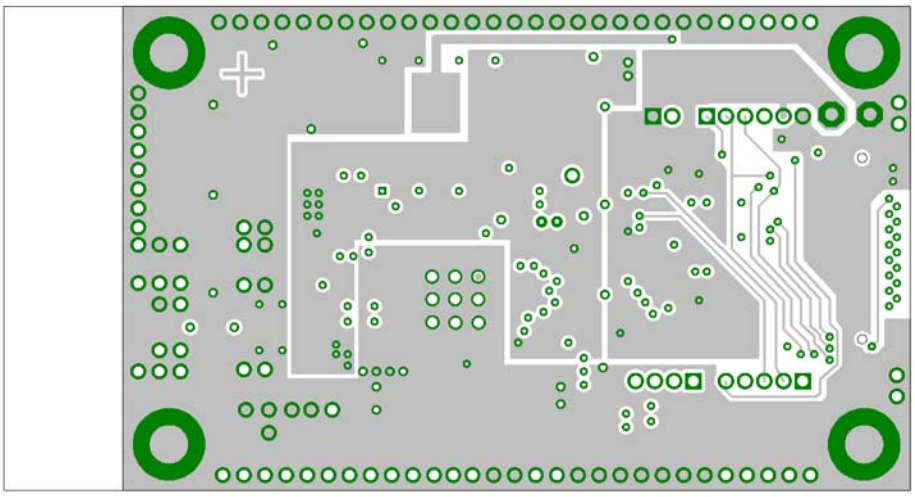


Figure 38: Reference design: bottom layer

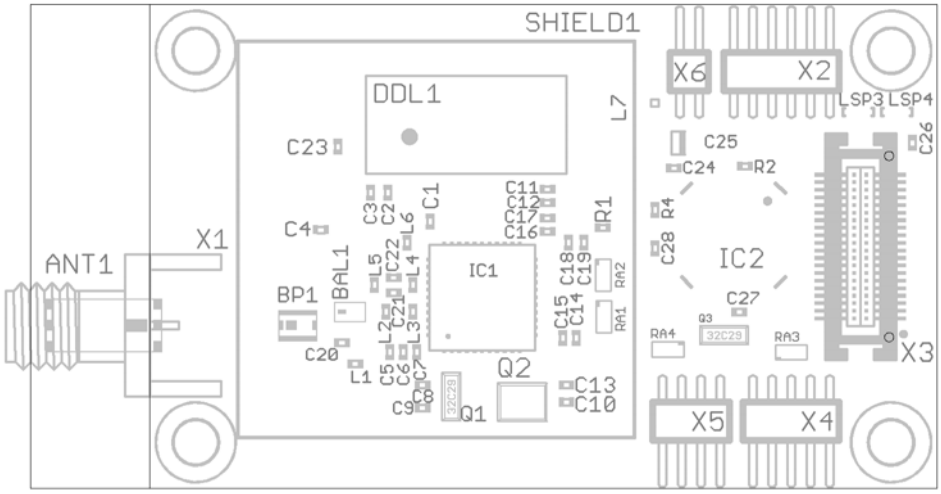


Figure 39: Reference design: top layer names

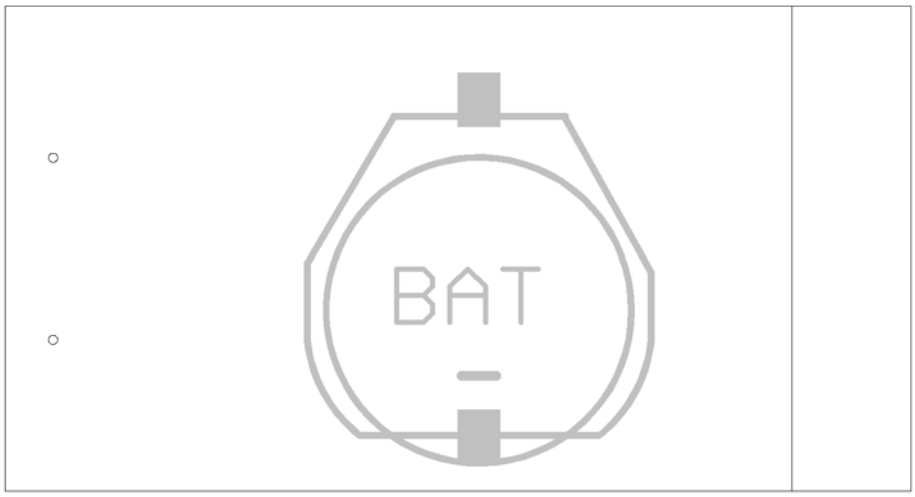


Figure 40: Reference design: bottom layer names (Inverted)

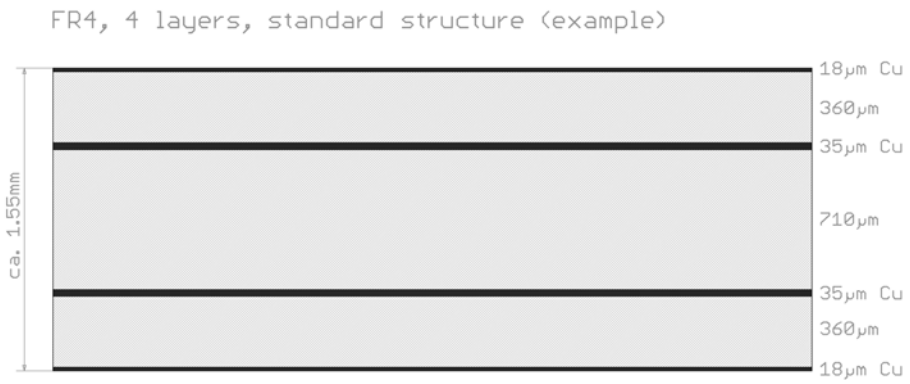


Figure 41: Reference design: layers, standard structure (example)

A1.1 Reference Design Bill of Materials

Table 11: Reference design bill of materials

Part					Manufacturer		Distributor	
Description	Label	Value	Qty	Package	Company	Product Number	Company	Order Number
Resistors	R1	100k	1	0402	PHYCOMP	2322 705 70104	Farnell	195-273
	R2, R4	10k	2	0402	MEGGITT	CRG0402J10K-10	Farnell	389-8659
	RA1	2k2	1	4R_ARRAY	PHYCOMP	ARV341 -2K2-5	Farnell	325-7447
	RA2	1M	1	4R_ARRAY	PHYCOMP	ARV341 -1M-5	Farnell	325-7605
	RA3	100k	1	4R_ARRAY	PHYCOMP	ARV341-100K-5	Farnell	325-7540
	RA4	220R	1	4R_ARRAY	PHYCOMP	ARV341 -220R-5	Farnell	325-7381
Capacitors	C15, C16	4.7pF	2	0402	PHYCOMP	2238 869 15478	Farnell	301-9147
	C21, C22	5.6pF	2	0402	Epcos	B37923K5050C660		
	C11	10pF	1	0402	AVX	CM05CG100D50AH	Farnell	578-058 (abgek.)
	C20	15pF	1	0402			Mira	8210/150
	C8, C9	22pF	2	0402	PHYCOMP	2238 869 15229	Farnell	301-9184
	C10, C13	27pF	2	0402			Mira	8210/270
	C1, C7, C18	100pF	3	0402	PHYCOMP	2238 869 15101	Farnell	301-9226
	C12	470pF	1	0402	PHYCOMP	2238 587 15618	Farnell	301-9366
	C2, C6	1nF	2	0402	PHYCOMP	2238 787 15636	Farnell	301-9380
	C3	10nF	1	0402	PHYCOMP	2238 587 15623	Farnell	301-9275
	C4, C5 C14, C17 C19, C23 C24, C26 C27, C28	100nF	10	0402	PHYCOMP	2238 787 19849	Farnell	301-9482
	C25	10uF/10V	1	3216	AVX	TAJA106K010R	Farnell	197-130
Inductors	L1	4.7nH	1	0402	Würth	744784047	Würth	744784047
	L2, L5	2.7nH	2	0402	Würth	744784027	Würth	744784027
	L3	6.8nH	1	0402	Würth	744765068	Würth	744765068
	L4	5.6nH	1	0402	Würth	744784056	Würth	744784056

Table 11: Reference design bill of materials

Part					Manufacturer		Distributor	
Description	**Label**	**Value**	**Qty**	**Package**	**Company**	**Product Number**	**Company**	**Order Number**
	L6	47nH	1	0402	Würth	74478447	Würth	74478447
	L7	742 792 69	1	0603	Würth	74279269	Würth	74279269
Balun	BAL1	50R:150R	1	BAL0805	Würth	748420245	Würth	748420245
Band pass filter	BP1	748351124	1	WE-BPF1008	Würth	748351124	Würth	748351124
SMD antenna	ANT1	WE-ANT20245	1	WE_ANT20245	Würth	7488920245	Würth	7488920245
CDDL	DDL1	CDDL_1804	1	13.3 X 6.5	Nanotron	DS1804C	Nanotron	DS1804C
Quartz	Q1, Q3	32.768kHz	2	31SMX	SMI	“31M327-12.5pF,20ppm”	DEQTRON	31M327 12.5pF, 20ppm
	Q2	16.0MHz	1	32SMX	SMI	“32 M 160-32 ,-40 ..+85°”	DEQTRON	32 M 160 -32, -40 ..+85°
Surface mount shield: 27x27x5.08	SHIELD1	SHIELD_BMIS_103	1	BMIS-103	Laird Technologies	BMIS-103	Laird Technologies	BMIS-103
surface mount coin cell holder: 20mm	BAT1	BAT_CLIP20	1	BAT_CLIP20	Keystone	1061	Farnell	302-9773
nanoNET transceiver	IC1	NA1TR8	1	VFQFPN7X7	Nanotron	NA1TR8	Nanotron	NA0108B
8-bit microcontroller	IC2	ATMEGA16L	1	MLF44	ATMEL	Atmega 16L-8MI	MSC	Atmega 16L-8MI
Connectors	X1	SMA-f	1	JOHNSON_JACK_GND_2	VITELEC	142-0701-851	RS Components	363-4690
	X2	06X1	1	CON_TMS_06X1_L_HEA	SAMTEC	TMS-106-03-G-S_RA	SAMTEC	TMS-106-01-G-S_RA
	X3	CON_DF17_40P_HEA	1	CON_DF17_40P_R05_HEA	HIROSE	DF17A(2.0)-40DP-0.5V(50)	MSC	DF17A(2.0)-40DP-0.5V(50)
	X4	05X1	1	CON_TMS_05X1_L_HEA	SAMTEC	TMS-105-03-G-S_RA	SAMTEC	TMS-105-01-G-S_RA
	X5	04X1	1	CON_TMS_04X1_L_HEA	SAMTEC	TMS-104-03-G-S_RA	SAMTEC	TMS-104-01-G-S_RA
	X6	02X1	1	CON_TMS_02X1_L_HEA	SAMTEC	TMS-102-03-G-S_RA	SAMTEC	TMS-102-01-G-S_RA

Revision History

Version	Date	Description/Changes
1.00	2003-10-11	Initial Release from internal document.
1.01	2003-12-16	Updated images, chip designations on page 19, 20.
1.02	2004-01-28	Bill of Materials table updated and package dimensions added.
1.03	2004-03-15	New template added, BOM updated, Example Application updated.
1.04	2004-04-08	Example application diagram updated, BOM updated, minor textual changes. Title changed to Datasheet.
2.00	2004-08-09	Pinning has changed from 48 pins to 44 pins. The Pin diagram and descriptions have been changed accordingly. Layout suggestion of CDDL connection added. Current consumption for TX changed to 78 *mA*. Other minor changes.
2.01	2004-09-10	Datasheet updated to latest data. Minor textual changes. Document sign-off table added.
2.02	2004-09-17	Example application updated. BOM table updated.
2.03	2004-11-05	Block diagram updated.
2.04	205-03-25	Parameters in this version for NA2TR1 chip. Nominal Conditions section added. General description updated. Modifications made to block diagram. Naming of Pin 2 and 3 corrected. Content of Absolute Maximum Ratings table modified. All parameters checked and reviewed. Example Application diagrams improved and updated. Both Bill of Materials tables modified. New section 10 added. Document status table added. Document status added.
2.05	2005-04-07	Chip values updated for NA1TR8. New feature: Programmable clock output at digital output.
2.06	2005-07-15	Template updated; Nominal conditions clarified (last point added); block diagram modified; term quartz oscillator used throughout; 32.768 kHz used throughout; V_{DDD}, V_{DDA} supply voltage typical added; Item 8.2.3 changed; timing diagrams added; output power graphs added; example application simplified and BOM deleted; new schematics and layout for recommended PCB layout for RF and IF part; RoHs directive data added; tape and reel information added; ordering information added; reference design appendix added. **Note**: The typical value for Item 8.1.10 supply current TX (P_{out} = *+8 dBm*) has been updated from 78 mA to 82 mA.
2.06	2005-07-15	Item 7.11 updated - description of pin clarified; clock signal provided by chip clarified; error corrected in SPI bus read timing diagram (SpiTxD);
2.07	2005-10-21	Minor textual changes; clarification of clock signal that can be provided by the chip (i.e., 32.768 kHz or from 125 kHz to 16 MHz); description of pin 11 VDDDCAP clarified; SpiTxD changed to SpiRxD in both Turn-on time RX and TX figures; error in SPI bus read timing figure fixed; Pin TxRx purpose clarified and elaborated; company address updated.
2.08	2006-11-10	Minor textual changes.

About Nanotron Technologies GmbH

Nanotron Technologies GmbH develops world-class wireless products for demanding applications based on its patented Chirp Spread Spectrum – an innovation that guarantees high robustness, optimal use of the available bandwidth, and low energy consumption. Since the beginning of 2005, Nanotron's Chirp technology has been a part of the IEEE 802.15.4a draft standard for wireless PANs which require extremely robust communication and low power consumption.

ICs and RF modules include the nanoNET TRX, the nanoLOC TRX, and ready-to-use or custom wireless solutions. These include, but are not limited to, industrial monitoring and control applications, medical applications (Active RFID), security applications, and Real Time Location Systems (RTLS). nanoNET is certified in Europe, United States, and Japan and supplied to customers worldwide.

Headquartered in Berlin, Germany, Nanotron Technologies GmbH was founded in 1991 and is an active member of IEEE, the ZigBee alliance, and ISA-SP100.

Further Information:

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