

MC14521B

24-Stage Frequency Divider

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to $2^{24} = 16,777,216$. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

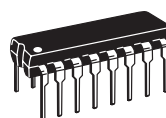
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



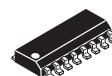
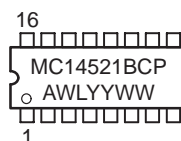
ON Semiconductor

<http://onsemi.com>

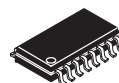
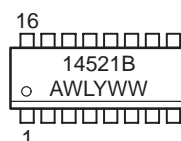
MARKING DIAGRAMS



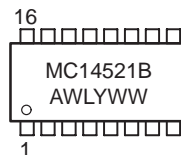
PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

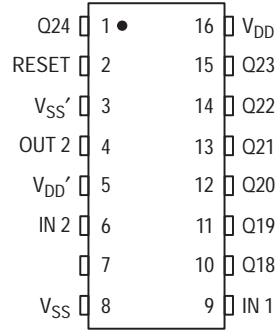
ORDERING INFORMATION

Device	Package	Shipping
MC14521BCP	PDIP-16	2000/Box
MC14521BD	SOIC-16	48/Rail
MC14521BDR2	SOIC-16	2500/Tape & Reel
MC14521BF	SOEIAJ-16	See Note 1.
MC14521BFEL	SOEIAJ-16	See Note 1.
MC14521BFR2	SOEIAJ-16	See Note 1.

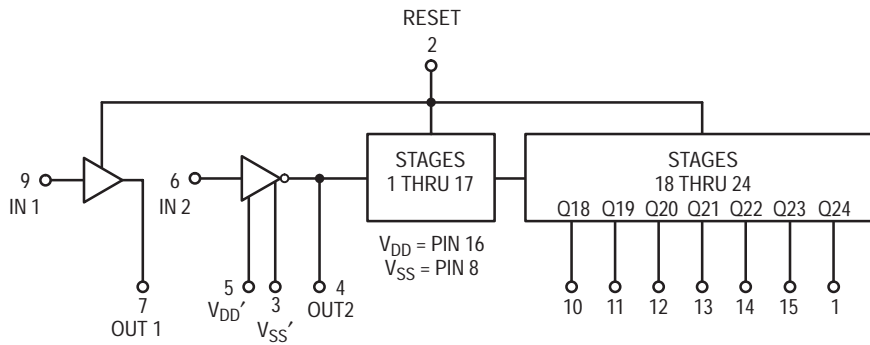
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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PIN ASSIGNMENT



BLOCK DIAGRAM



Output	Count Capacity
Q18	$2^{18} = 262,144$
Q19	$2^{19} = 524,288$
Q20	$2^{20} = 1,048,576$
Q21	$2^{21} = 2,097,152$
Q22	$2^{22} = 4,194,304$
Q23	$2^{23} = 8,388,608$
Q24	$2^{24} = 16,777,216$

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD}	"0" Level V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) "1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current ($V_{OH} = 2.5$ Vdc) Source ($V_{OH} = 4.6$ Vdc) Pins 4 & 7 ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OH} = 2.5$ Vdc) Source ($V_{OH} = 4.6$ Vdc) Pins 1, 10, ($V_{OH} = 9.5$ Vdc) 11, 12, 13, 14 ($V_{OH} = 13.5$ Vdc) and 15 ($V_{OL} = 0.4$ Vdc) Sink ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	I_{OH}	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc	
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—		
		10	-0.62	—	-0.5	-0.9	—	-0.35	—		
		15	-1.8	—	-1.5	-3.5	—	-1.1	—		
		5.0	-3.0	—	-2.4	-4.2	—	-1.7	—		mAdc
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
		5.0	—	—	—	—	—	—	—		mAdc
		5.0	—	—	—	—	—	—	—		
		5.0	—	—	—	—	—	—	—		—
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μ Adc	
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μ Adc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.42 \mu\text{A/kHz}) f + I_{DD}$							μ Adc	
		10	$I_T = (0.85 \mu\text{A/kHz}) f + I_{DD}$								
		15	$I_T = (1.40 \mu\text{A/kHz}) f + I_{DD}$								

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.003$.

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SWITCHING CHARACTERISTICS (7.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (8.)	Max	Unit
Output Rise and Fall Time (Counter Outputs) $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q18 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 4415 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 1667 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1275 \text{ ns}$ Clock to Q24 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 2167 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 1675 \text{ ns}$	t_{PHL}, t_{PLH}	5.0 10 15 5.0 10 15	— — — — — —	4.5 1.7 1.3 6.0 2.2 1.7	9.0 3.5 2.7 12 4.5 3.5	μs
Propagation Delay Time Reset to Q_n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1215 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 467 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 350 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	1300 500 375	2600 1000 750	ns
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	385 150 120	140 55 40	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	3.5 9.0 12	2.0 5.0 6.5	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	μs
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	1400 600 450	700 300 225	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	30 0 -40	-200 -160 -110	— — —	ns

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

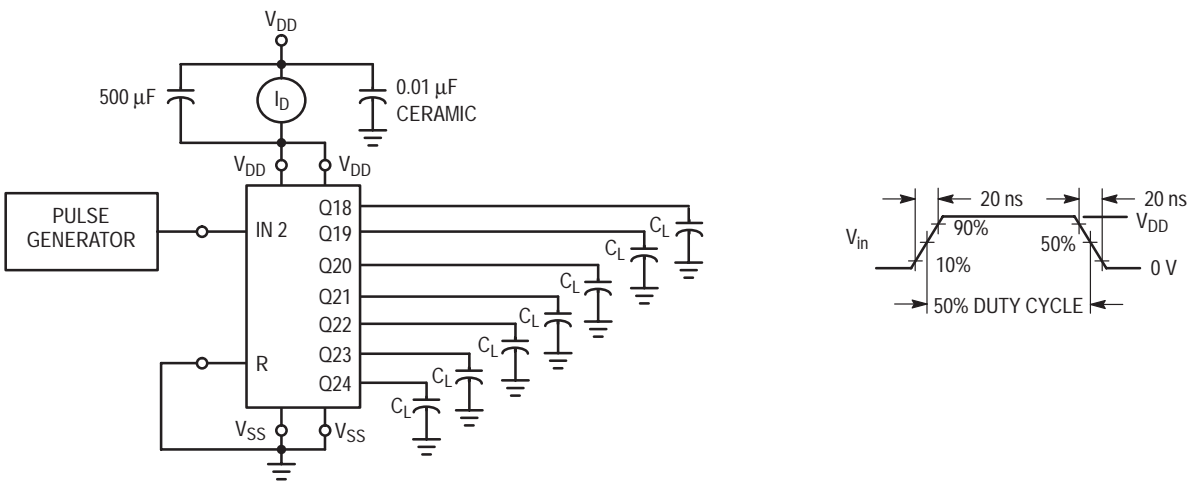


Figure 1. Power Dissipation Test Circuit and Waveform

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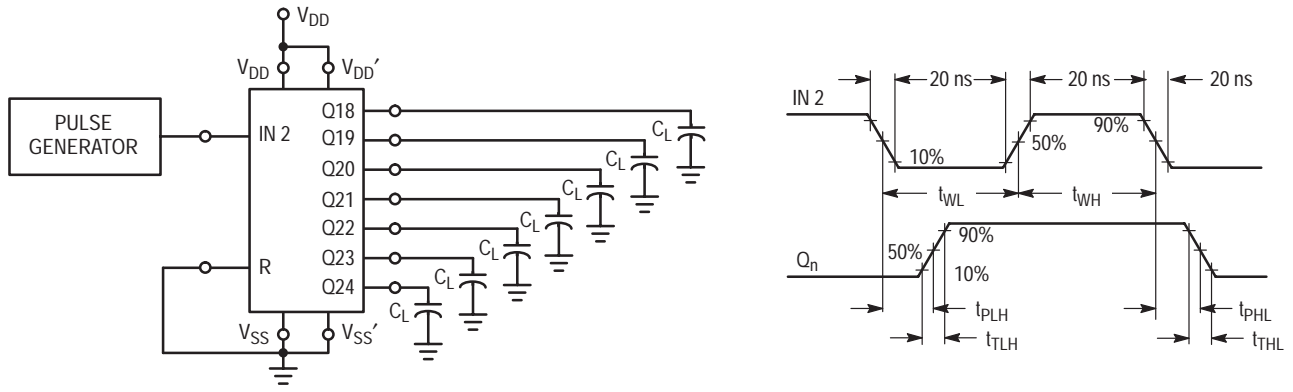
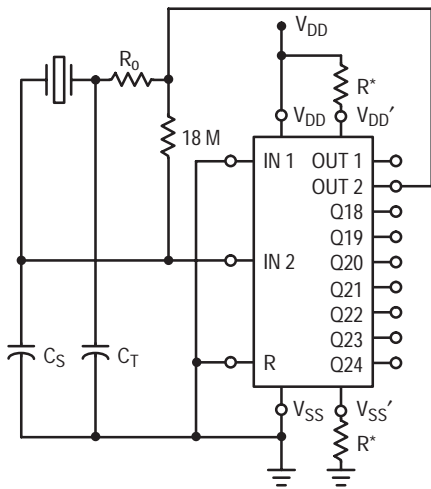


Figure 2. Switching Time Test Circuit and Waveforms



* Optional for low power operation,
 $10 \text{ k}\Omega \leq R \leq 70 \text{ k}\Omega$.

Figure 3. Crystal Oscillator Circuit

Characteristic	500 kHz Circuit	50 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	$\text{k}\Omega$
External Resistor/Capacitor Values			
R_o	47	750	$\text{k}\Omega$
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} ($T_A = 25^\circ\text{C}$)			
V_{DD} Change from 5.0 V to 10 V	+ 6.0	+ 2.0	ppm
V_{DD} Change from 10 V to 15 V	+ 2.0	+ 2.0	ppm
Frequency Change as a Function of Temperature ($V_{DD} = 10 \text{ V}$)			
T_A Change from -55°C to $+25^\circ\text{C}$	- 4.0	- 2.0	ppm
MC14521 only	+ 100	+ 120	ppm
Complete Oscillator*			
T_A Change from $+25^\circ\text{C}$ to $+125^\circ\text{C}$	- 2.0	- 2.0	ppm
MC14521 only	- 160	- 560	ppm
Complete Oscillator*			

*Complete oscillator includes crystal, capacitors, and resistors.

Figure 4. Typical Data for Crystal Oscillator Circuit

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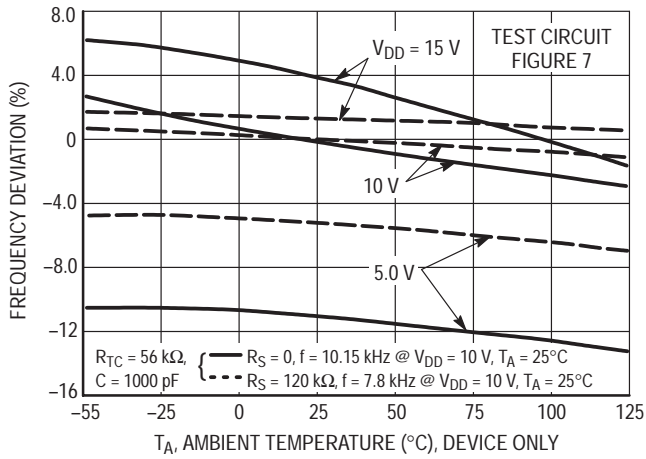


Figure 5. RC Oscillator Stability

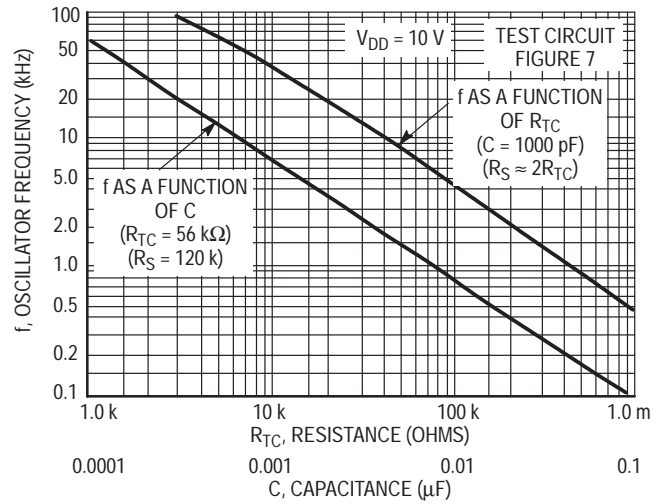


Figure 6. RC Oscillator Frequency as a Function of R_{TC} and C

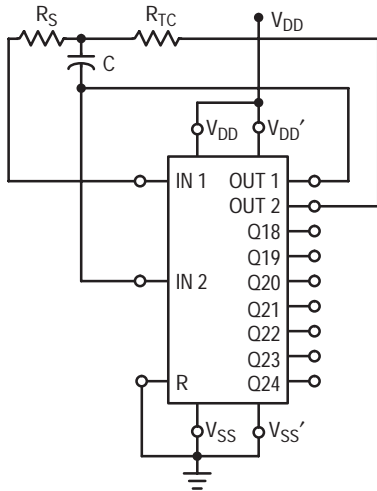


Figure 7. RC Oscillator Circuit

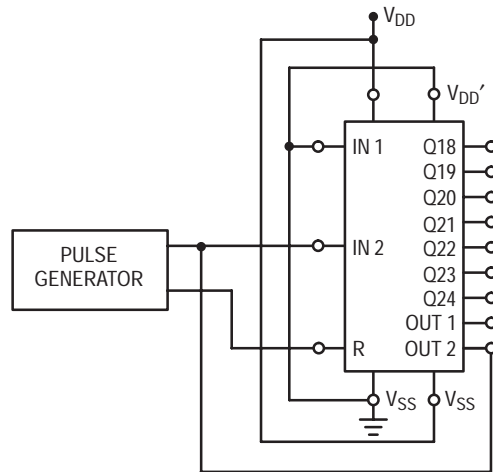


Figure 8. Functional Test Circuit

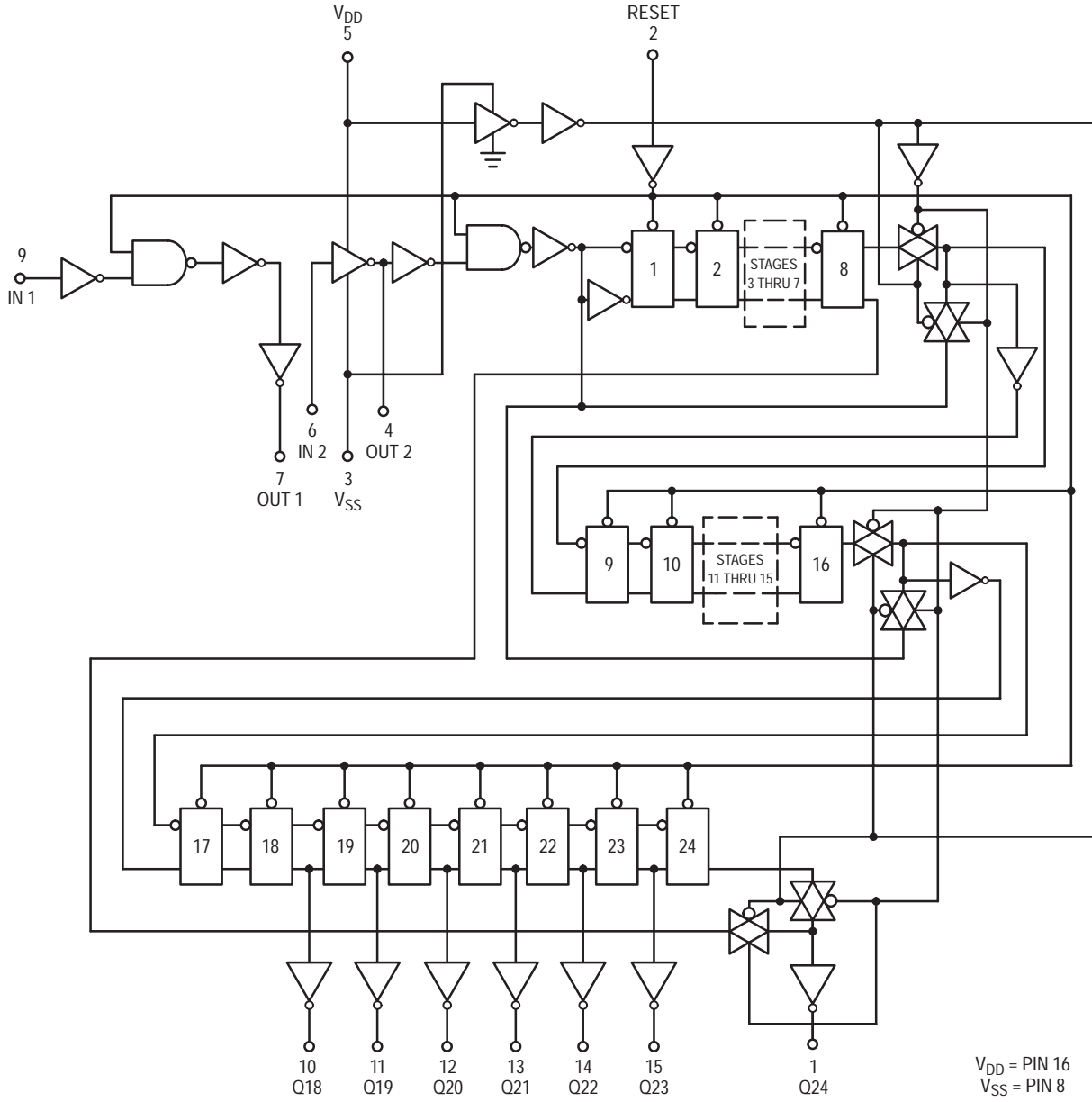
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FUNCTIONAL TEST SEQUENCE

	Inputs		Outputs			Comments			
	Reset	In 2	Out 2	V _{SS} '	V _{DD} '		Q18 thru Q24		
<p>A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.</p>	1	0	0	V _{DD}	Gnd	0	Counter is in three 8-stage sections in parallel mode. Counter is reset. In 2 and Out 2 are connected together.		
	0	1	1			0	First "0" to "1" transition on In 2, Out 2 node.		
	0	0	0			1	255 "0" to "1" transitions are clocked into this In 2, Out 2 node.		
	1	1	1			1	The 255th "0" to "1" transition.		
	0	0	0			1	1		
	1	0	0			1	1	Counter converted back to 24-stages in series mode.	
	1	0	0			1	1	Out 2 converts back to an output.	
	0	1	1			1	1	Counter ripples from an all "1" state to an all "0" stage.	
	0	0	0			Gnd	V _{DD}	0	
	0	1	1			Gnd	V _{DD}	0	

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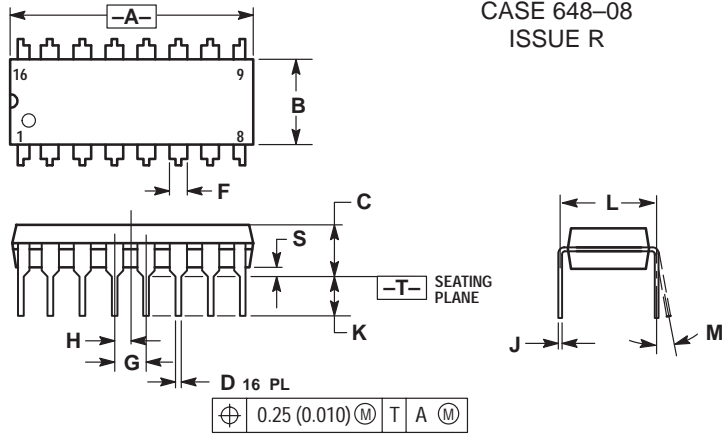
LOGIC DIAGRAM



MC14521B

PACKAGE DIMENSIONS

PDIP-16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE R



NOTES:

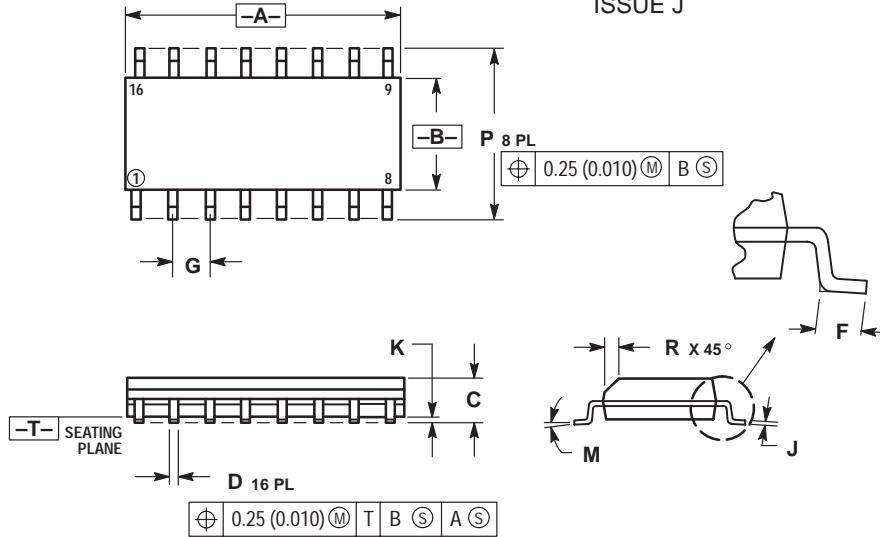
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

MC14521B

PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



NOTES:

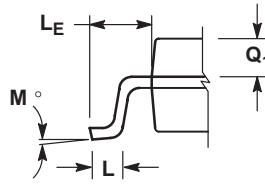
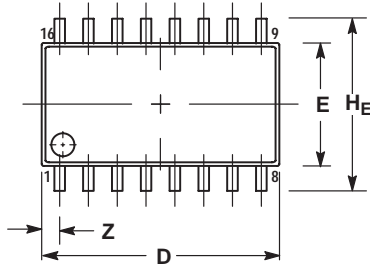
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

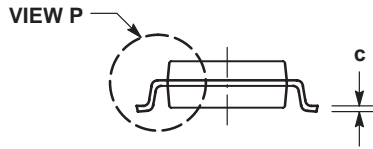
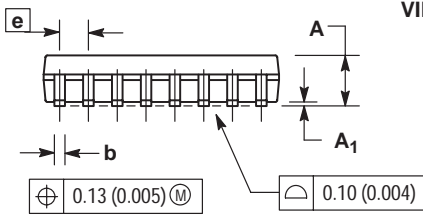
MC14521B

PACKAGE DIMENSIONS

SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _F	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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