

## 1.8V Input/Output Rail-to-Rail Low Power Operational Amplifiers

- Operating at  $V_{CC} = 1.8V$  to  $6V$
- Rail-to-rail input & output
- Extended  $V_{ICM}$  ( $V_{DD} - 0.2V$  to  $V_{CC} + 0.2V$ )
- Low supply current ( $400\mu A$ )
- Gain bandwidth product (1.6MHz)
- High stability
- ESD tolerance (2kV)
- Latch-up immunity
- Available in SOT23-5 micropackage

### Description

The TS187x (single, dual & quad) is an operational amplifier family able to operate with voltage as low as 1.8V and features both I/O rail-to-rail.

The common mode input voltage extends 200mV at  $25^\circ C$  beyond the supply voltages while the output voltage swing is within 100mV of each rail with 600 Ohm load resistor. This device consumes typically  $400\mu A$  per channel while offering 1.6Mhz of gain-bandwidth product. The amplifier provides high output drive capability typically at 65mA-load.

These performances make the TS187X family ideal for sensor interface, battery-supplied and portable applications.

### Applications

- Battery-powered applications (toys)
- Portable communication devices (cell phone)
- Audio driver (headphone driver)
- Laptop/notebook computers

### Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS1871ID/IDT/AID/AIDT	$-40^\circ C$ , $+125^\circ C$	SO	Tube or Tape & Reel	
TS1871ILT/AILT		SOT23-5L	Tape & Reel	K171/K172
TS1872IN/AIN		DIP	Tube	
TS1872ID/IDT/AID/AIDT		SO	Tube or Tape & Reel	
TS1872IPT/AIPT		TSSOP (Thin Shrink Outline Package)	Tape & Reel	
TS1872IST/AIST		mini SO	Tape & Reel	K171/K172
TS1874IN/AIN		DIP	Tube	
TS1874ID/IDT/AID/AIDT		SO	Tube or Tape & Reel	
TS1874IPT/AIPT		TSSOP (Thin Shrink Outline Package)	Tape & Reel	

## 1 Absolute Maximum Ratings

**Table 1: Key parameters and their absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>1</sup>	7	V
$V_{id}$	Differential Input Voltage <sup>2</sup>	$\pm 1$	V
$V_i$	Input Voltage	$V_{DD}-0.3$ to $V_{CC}+0.3$	V
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_j$	Maximum Junction Temperature	150	°C
$R_{thja}$	Thermal Resistance Junction to Ambient <sup>3</sup> SOT23-5 SO8 SO14 TSSOP8 TSSOP14 miniSO8	250 125 103 120 100 190	°C/W
ESD	HBM: Human Body Model <sup>4</sup>	2	kV
	MM: Machine Model <sup>5</sup>	200	V
	CDM: Charged Device Model	1.5	kV
	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	250	°C
	Output Short Circuit Duration	see note <sup>6</sup>	

- 1) All voltages values, except differential voltage are with respect to network terminal.
- 2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. If  $V_{id} > \pm 1V$ , the maximum input current must not exceed  $\pm 1mA$ . In this case ( $V_{id} > \pm 1V$ ) an input series resistor must be added to limit input current.
- 3) Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuit on all amplifiers
- 4) Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
- 5) Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor  $< 5\Omega$ ), into pin to pin of device.
- 6) Short-circuits from the output to  $V_{CC}$  can cause excessive heating. The maximum output current is approximately 80mA, independent of the magnitude of  $V_{CC}$ . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

**Table 2: Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	1.8 to 6	V
$V_{icm}$	Common Mode Input Voltage Range <sup>1</sup>	$V_{DD} - 0.2$ to $V_{CC} + 0.2$	V
$V_{icm}$	Common Mode Input Voltage Range <sup>2</sup>	$V_{DD}$ to $V_{CC}$	V
$T_{oper}$	Operating Free Air Temperature Range	-40 to + 125	°C

- 1) At 25°C, for  $1.8 \leq V_{CC} \leq 6V$ ,  $V_{icm}$  is extended to  $V_{DD} - 0.2V$ ,  $V_{CC} + 0.2V$ .
- 2) In full temperature range, both Rails can be reached when  $V_{CC}$  does not exceed 5.5V.

## 2 Electrical Characteristics

Table 3:  $V_{CC} = +1.8V$ ,  $V_{DD} = 0V$ ,  $R_L$ ,  $C_L$  connected to  $V_{CC}/2$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage $V_{icm} = V_{out} = V_{CC}/2$ TS1871/2/4 TS1871A/2A/4A		0.1	3 1	mV
$\Delta V_{io}$	Input Offset Voltage Drift		2		$\mu V/^\circ C$
$I_{io}$	Input Offset Current <sup>1)</sup> $V_{icm} = V_{out} = V_{CC}/2$		3	30	nA
$I_{ib}$	Input Bias Current <sup>1)</sup> $V_{icm} = V_{out} = V_{CC}/2$		40	125	nA
CMR	Common Mode Rejection Ratio $0 \leq V_{icm} \leq V_{CC}$ , $V_{out} = V_{CC}/2$	55	77		dB
SVR	Supply Voltage Rejection Ratio	70	80		dB
$A_{vd}$	Large Signal Voltage Gain $V_{out} = 0.5V$ to $1.3V$ $R_L = 2k\Omega$ $R_L = 600\Omega$	77 70	92 85		dB
$V_{OH}$	High Level Output Voltage $V_{id} = 100mV$ $R_L = 2k\Omega$ $R_L = 600\Omega$	1.65 1.62	1.77 1.74		V
$V_{OL}$	Low Level Output Voltage $V_{id} = -100mV$ $R_L = 2k\Omega$ $R_L = 600\Omega$		88 115	100 150	mV
$I_o$	Output Source Current $V_{ID} = 100mV$ , $V_O = V_{DD}$ Output Sink Current $V_{ID} = -100mV$ , $V_O = V_{CC}$	20 20	65 65		mA
$I_{cc}$	Supply Current (per amplifier), $V_{out} = V_{CC}/2$ $A_{VCL} = 1$ , no load		400	560	$\mu A$
GBP	Gain Bandwidth Product $R_L = 10k\Omega$ , $C_L = 100pF$ , $f = 100kHz$	0.9	1.6		MHz
SR	Slew Rate $R_L = 10k\Omega$ , $C_L = 100pF$ , $AV = 1$	0.38	0.54		V/ $\mu s$
$\phi_m$	Phase Margin $C_L = 100pF$		53		Degrees
en	Input Voltage Noise		27		$nV/\sqrt{Hz}$
THD	Total Harmonic Distortion		0.01		%

1) Maximum values including unavoidable inaccuracies of the industrial test.

**Table 4:  $V_{CC} = +3V$ ,  $V_{DD} = 0V$ ,  $R_L$ ,  $C_L$  connected to  $V_{CC}/2$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage $V_{icm} = V_{out} = V_{CC}/2$ TS1871/2/4 TS1871A/2A/4A		0.1	3 1	mV
$\Delta V_{io}$	Input Offset Voltage Drift		2		$\mu V/^\circ C$
$I_{io}$	Input Offset Current <sup>1)</sup> $V_{icm} = V_{out} = V_{CC}/2$		3	30	nA
$I_{ib}$	Input Bias Current <sup>1)</sup> $V_{icm} = V_{out} = V_{CC}/2$		4	125	nA
CMR	Common Mode Rejection Ratio $0 \leq V_{icm} \leq V_{CC}$ , $V_{out} = V_{CC}/2$	60	80		dB
SVR	Supply Voltage Rejection Ratio	70	85		dB
$A_{vd}$	Large Signal Voltage Gain $V_{out} = 0.5V$ to $2.5V$ $R_L = 2k\Omega$ $R_L = 600\Omega$	80 74	92 95		dB
$V_{OH}$	High Level Output Voltage $V_{id} = 100mV$ $R_L = 2k\Omega$ $R_L = 600\Omega$	2.82 2.80	2.95 2.95		V
$V_{OL}$	Low Level Output Voltage $V_{id} = -100mV$ $R_L = 2k\Omega$ $R_L = 600\Omega$		88 115	L120 160	mV
$I_o$	Output Source Current $V_{ID} = 100mV$ , $V_O = V_{DD}$ Output Sink Current $V_{ID} = -100mV$ , $V_O = V_{CC}$	20 20	80 80		mA
$I_{cc}$	Supply Current (per amplifier), $V_{out} = V_{CC}/2$ $A_{VCL} = 1$ , no load		450	650	$\mu A$
GBP	Gain Bandwidth Product $R_L = 10k\Omega$ , $C_L = 100pF$ , $f = 100kHz$	1	1.7		MHz
SR	Slew Rate $R_L = 10k\Omega$ , $C_L = 100pF$ , $AV = 1$	0.42	0.6		V/ $\mu s$
$\phi_m$	Phase Margin $C_L = 100pF$		53		Degrees
en	Input Voltage Noise		27		$nV/\sqrt{Hz}$
THD	Total Harmonic Distortion		0.01		%

1) Maximum values including unavoidable inaccuracies of the industrial test.

**Table 5:  $V_{CC} = +5V$ ,  $V_{DD} = 0V$ ,  $C_L$  &  $R_L$  connected to  $V_{CC}/2$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage $V_{icm} = V_{out} = V_{CC}/2$ TS1871/2/4 TS1871A/2A/4A		0.1	3 1	mV
$\Delta V_{io}$	Input Offset Voltage Drift		2		$\mu V/^\circ C$
$I_{io}$	Input Offset Current <sup>1)</sup> $V_{icm} = V_{out} = V_{CC}/2$		3	30	nA
$I_{ib}$	Input Bias Current <sup>1)</sup> $V_{icm} = V_{out} = V_{CC}/2$		70	130	nA
CMR	Common Mode Rejection Ratio $0 \leq V_{icm} \leq V_{CC}$ , $V_{out}$ different of $V_{CC}/2$	65	85		dB
SVR	Supply Voltage Rejection Ratio	70	90		dB
$A_{vd}$	Large Signal Voltage Gain $V_{out} = 1V$ to $4V$ $R_L = 2k\Omega$ $R_L = 600\Omega$	83 77	92 85		dB
$V_{OH}$	High Level Output Voltage $V_{id} = 100mV$ $R_L = 2k\Omega$ $R_L = 600\Omega$	4.80 4.75	4.95 4.90		V
$V_{OL}$	Low Level Output Voltage $V_{id} = -100mV$ $R_L = 2k\Omega$ $R_L = 600\Omega$		88 115	130 188	mV
$I_o$	Output Source Current $V_{ID} = 100mV$ , $V_O = V_{DD}$ Output Sink Current $V_{ID} = -100mV$ , $V_O = V_{CC}$	20 20	80 80		mA
$I_{cc}$	Supply Current (per amplifier), $V_{out} = V_{CC}/2$ $A_{VCL} = 1$ , no load		500	835	$\mu A$
GBP	Gain Bandwidth Product $R_L = 10k\Omega$ , $C_L = 100pF$ , $f = 100kHz$	1	1.8		MHz
SR	Slew Rate $R_L = 10k\Omega$ , $C_L = 100pF$ , $AV = 1$	0.42	0.6		V/ $\mu s$
$\phi_m$	Phase Margin $C_L = 100pF$		55		Degrees
en	Input Voltage Noise		27		$nV/\sqrt{Hz}$
THD	Total Harmonic Distortion		0.01		%

1) Maximum values including unavoidable inaccuracies of the industrial test.

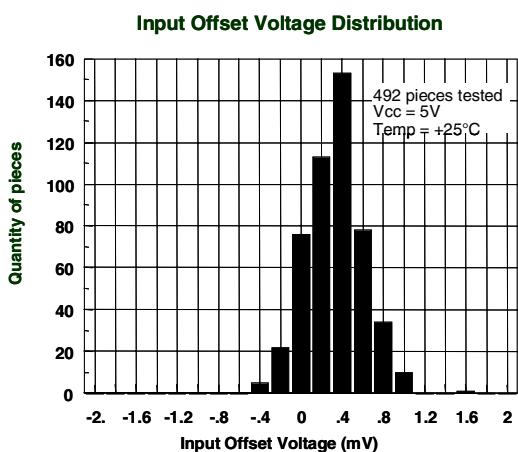
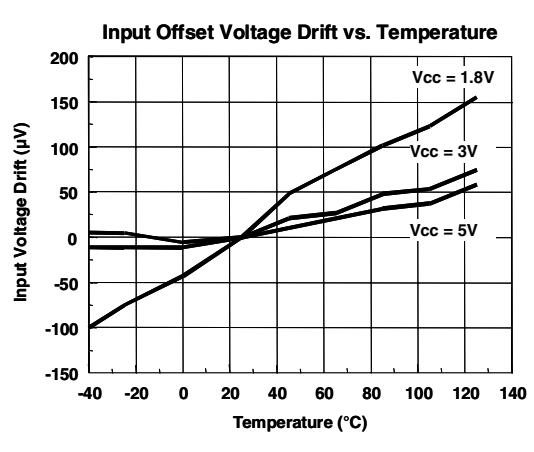
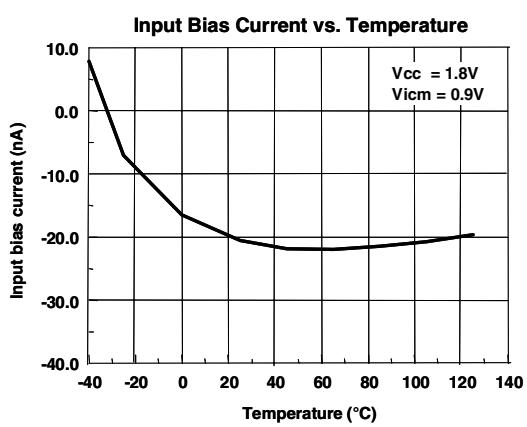
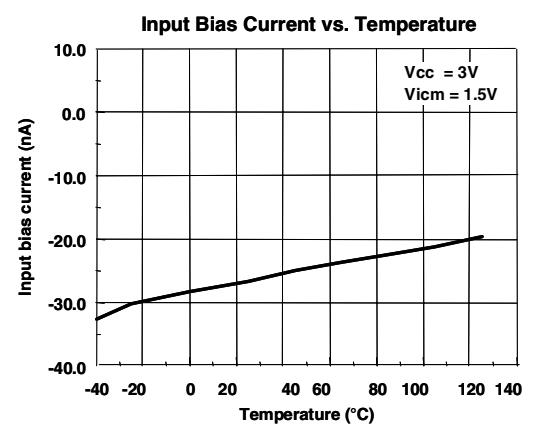
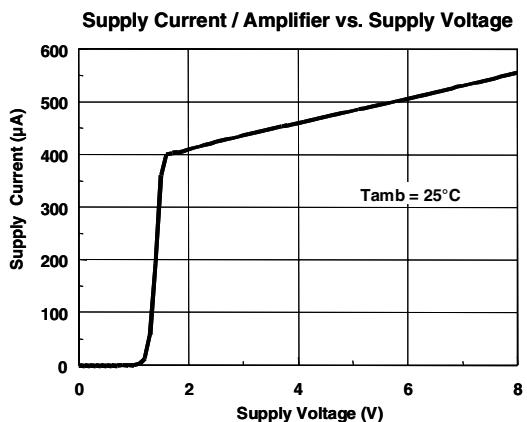
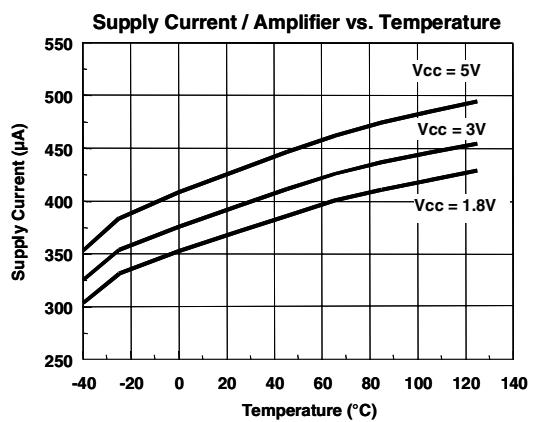
**Figure 1 :****Figure 4 :****Figure 2 :****Figure 5 :****Figure 3 :****Figure 6 :**

Figure 7 :

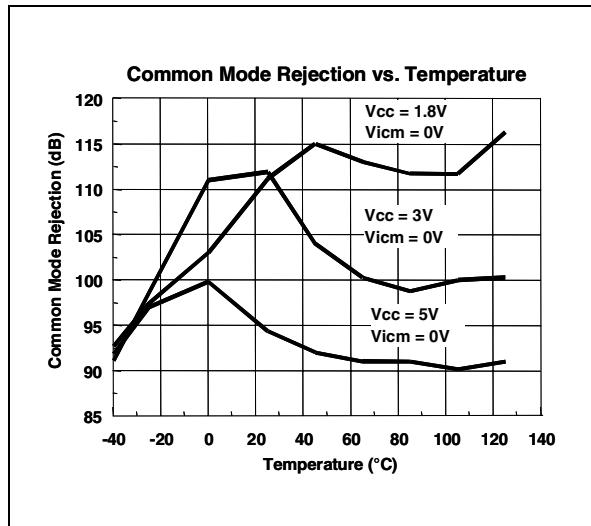


Figure 10 :

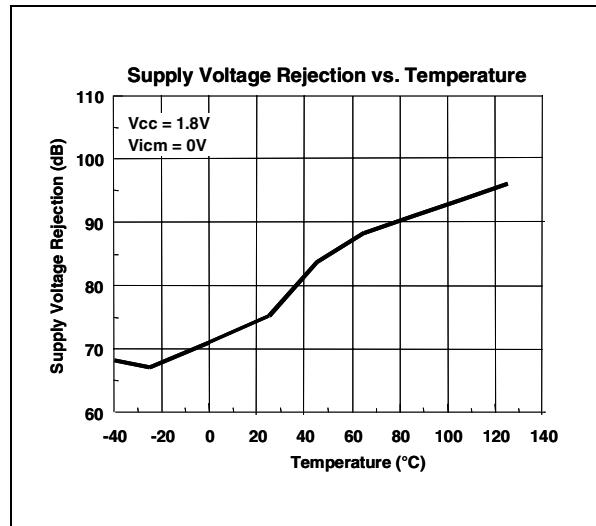


Figure 8 :

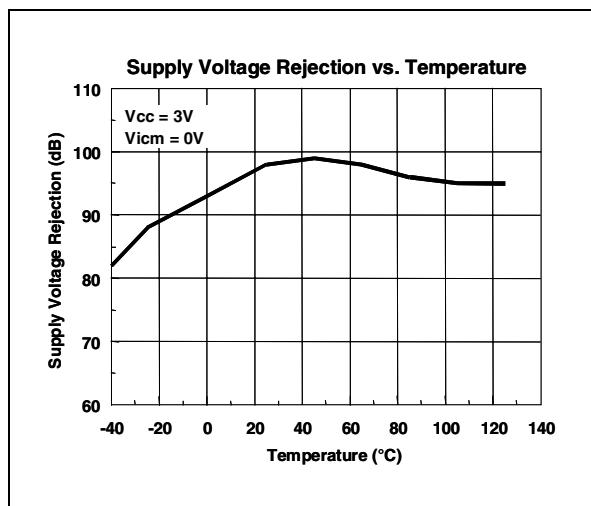


Figure 11 :

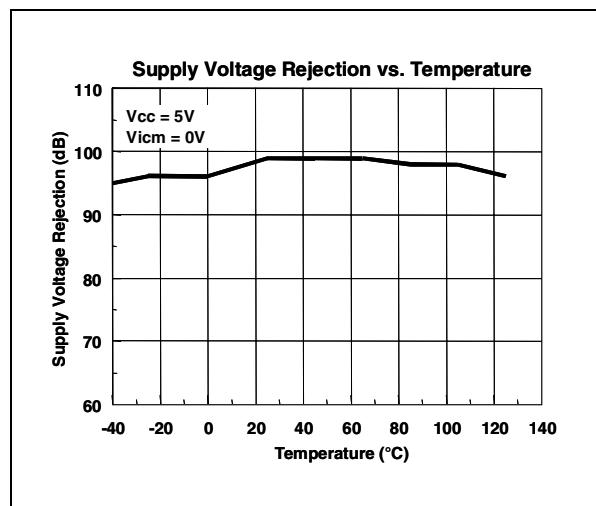


Figure 9 :

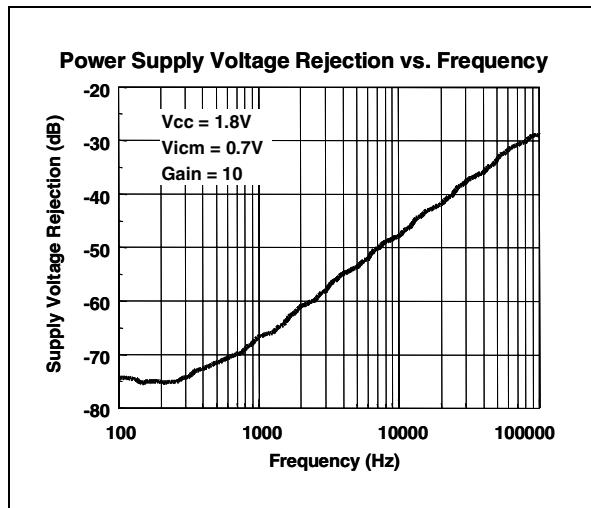


Figure 12 :

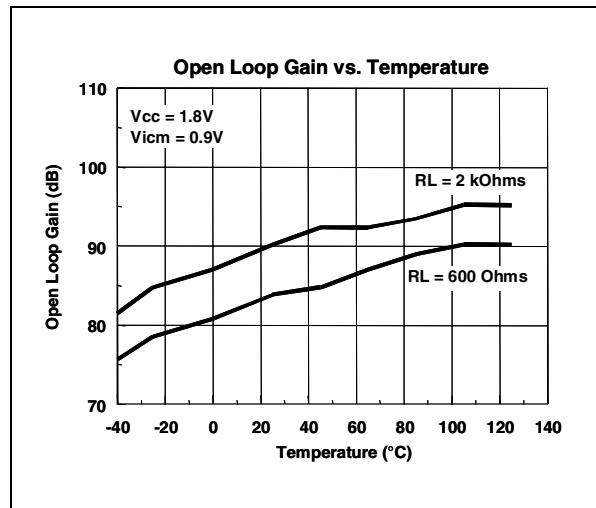


Figure 13 :

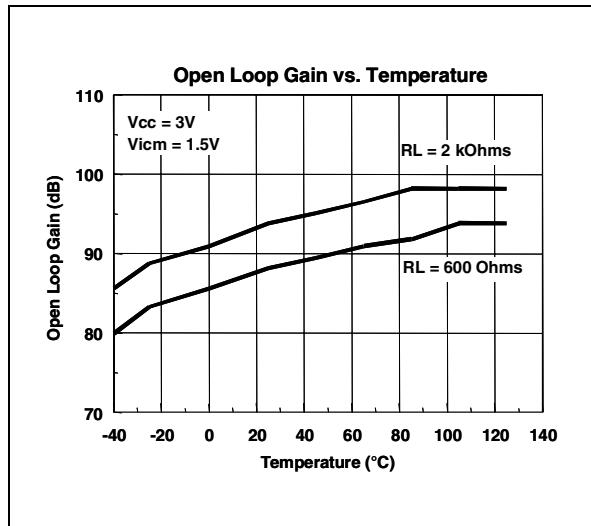


Figure 16 :

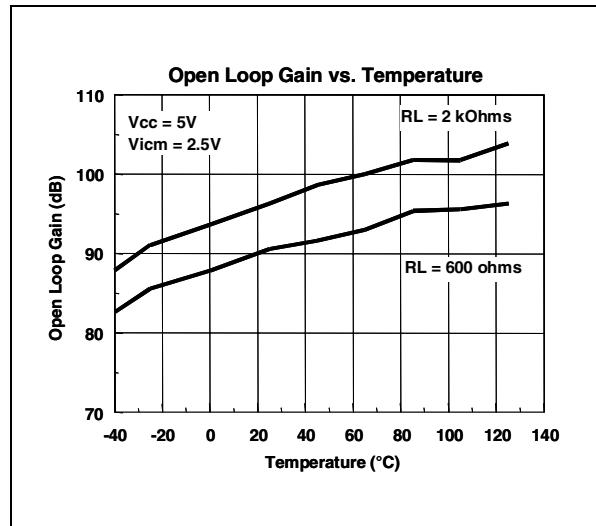


Figure 14 :

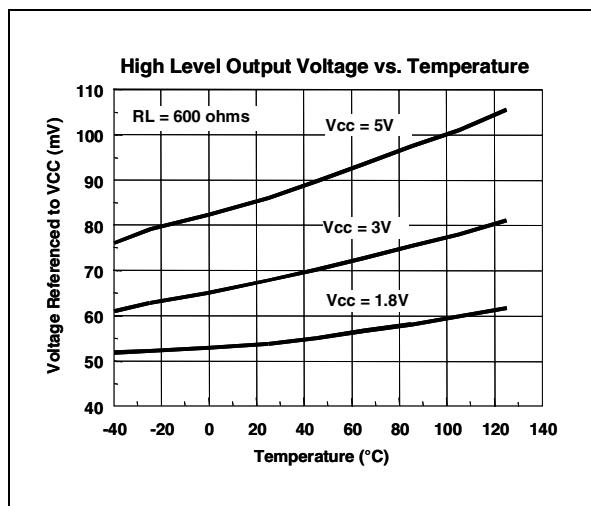


Figure 17 :

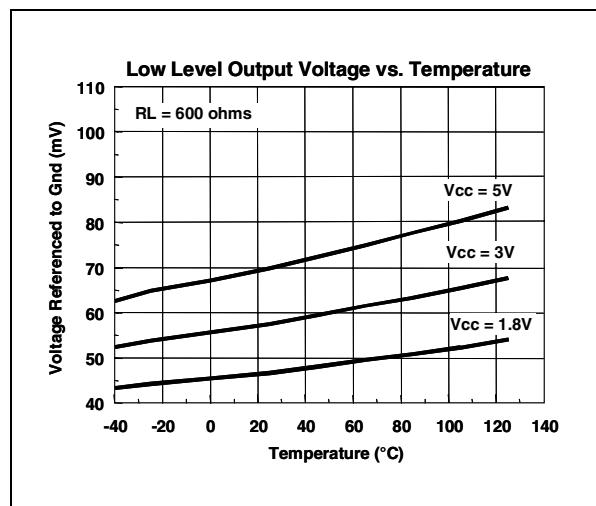


Figure 15 :

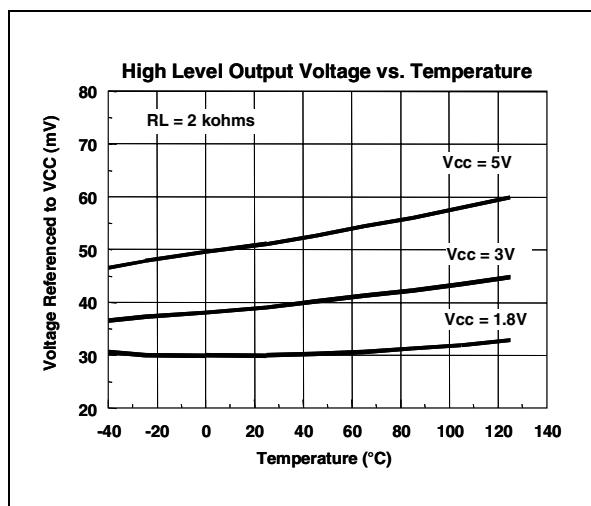


Figure 18 :

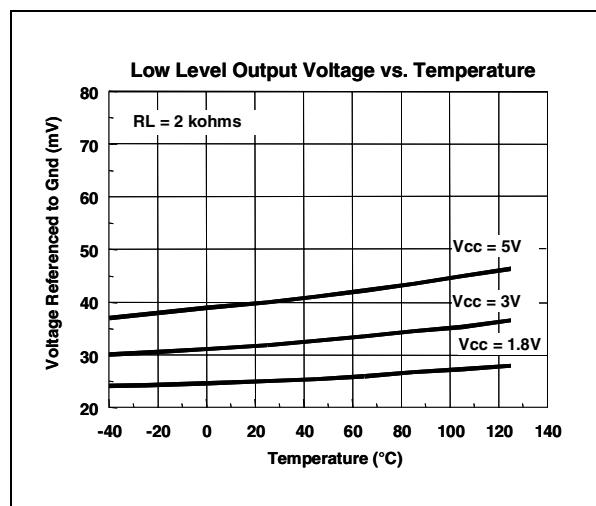


Figure 19 :

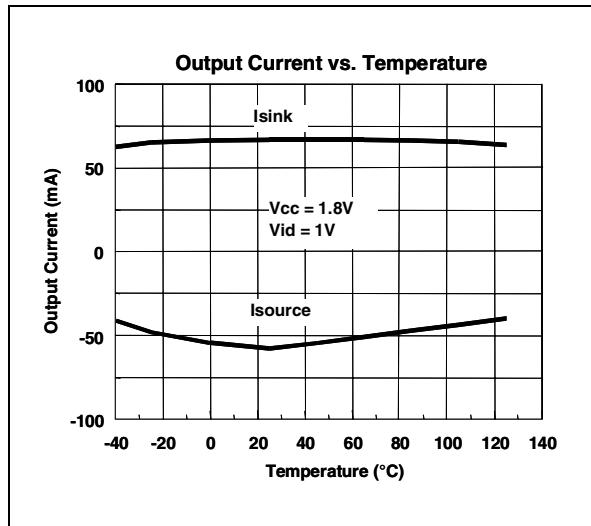


Figure 22 :

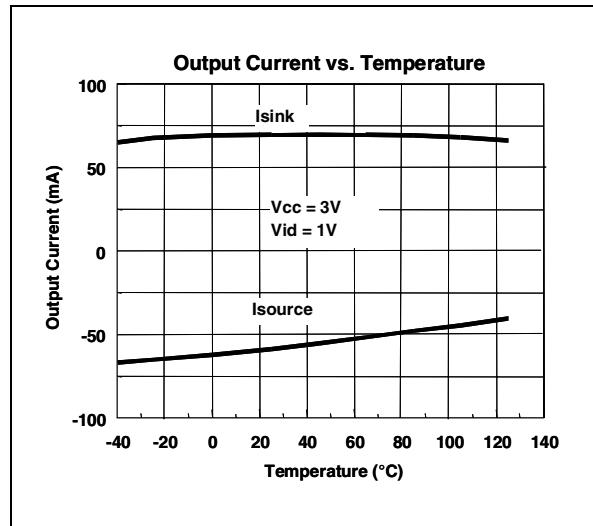


Figure 20 :

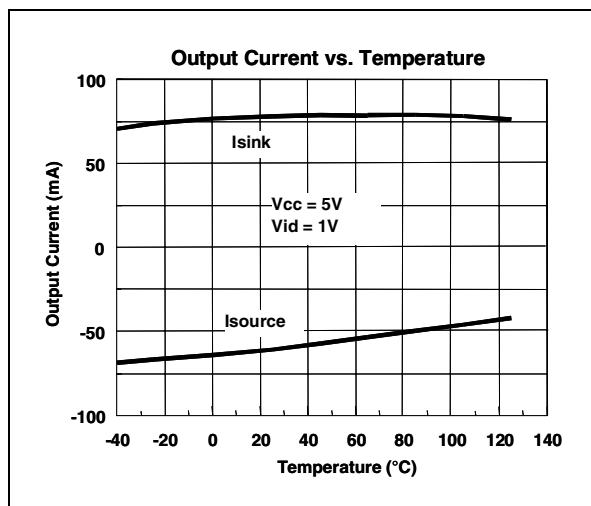


Figure 23 :

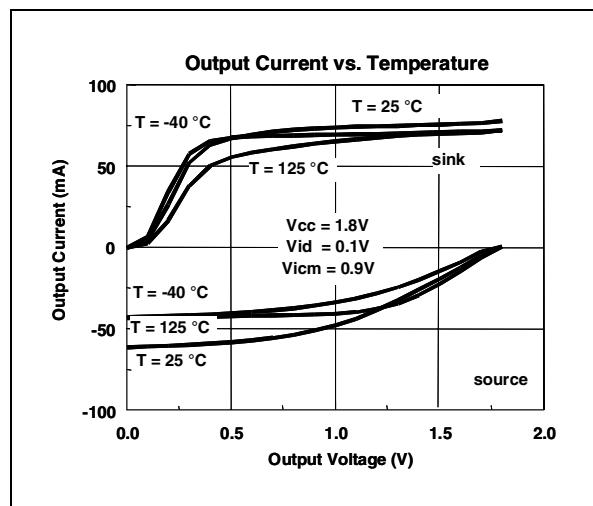


Figure 21 :

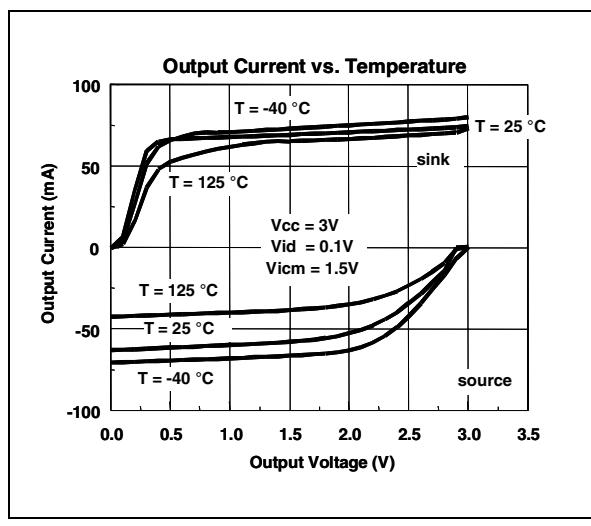


Figure 24 :

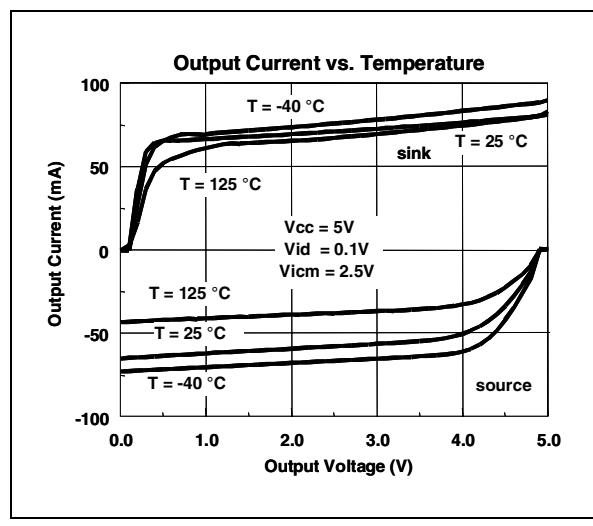


Figure 25 :

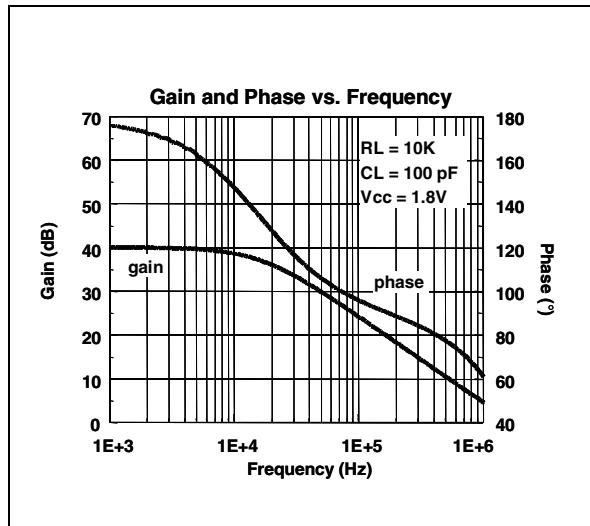


Figure 28 :

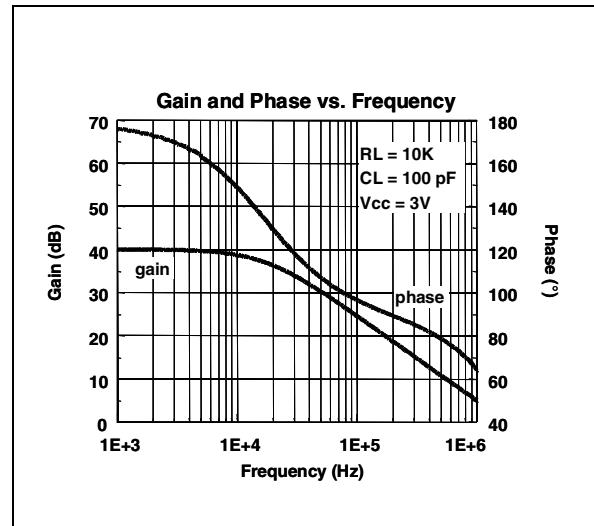


Figure 26 :

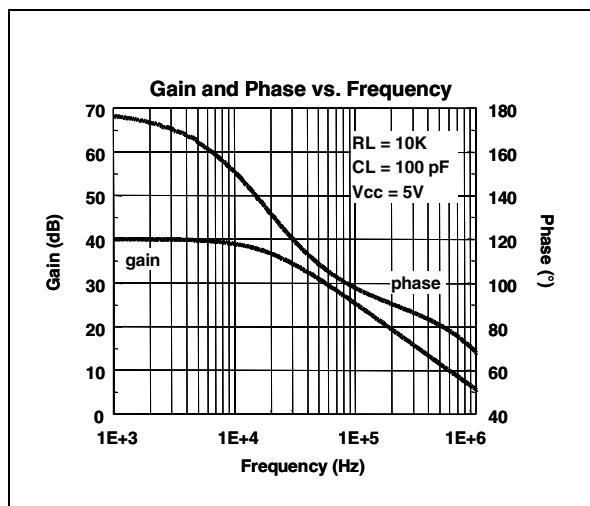


Figure 29 :

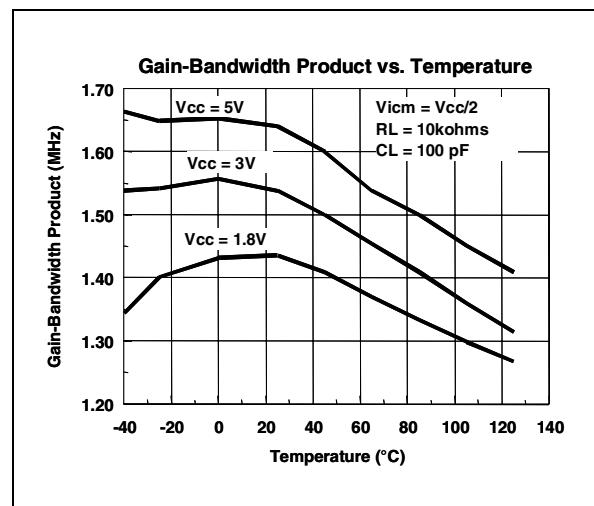


Figure 27 :

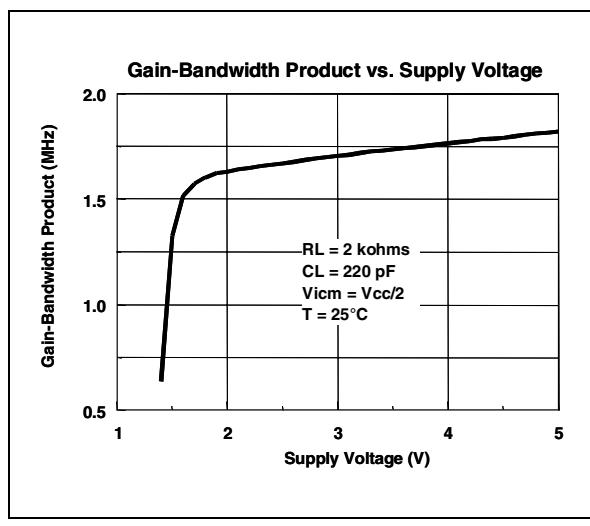


Figure 30 :

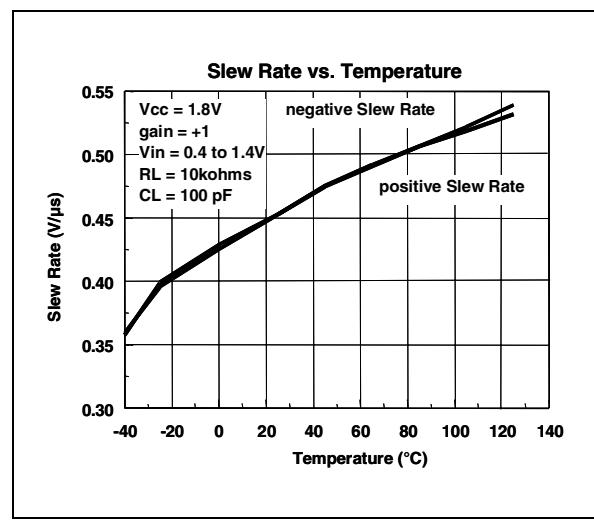


Figure 31 :

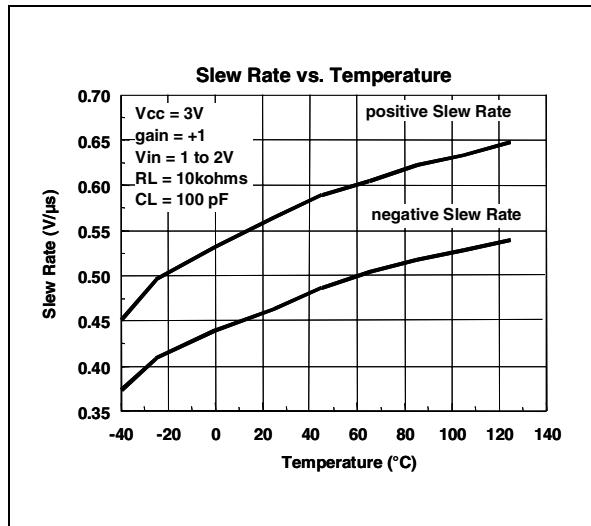


Figure 34 :

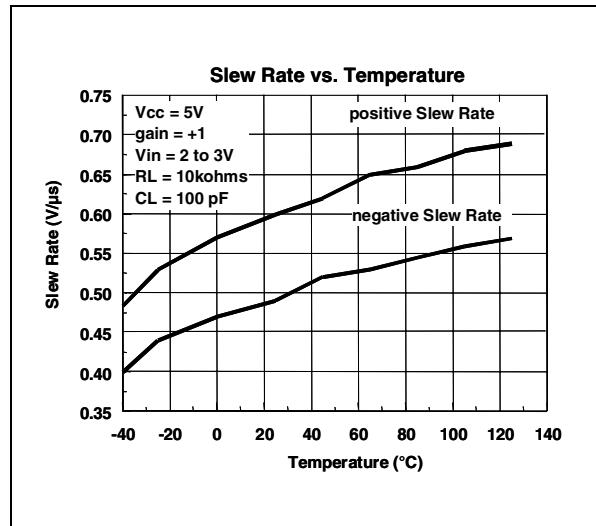


Figure 32 :

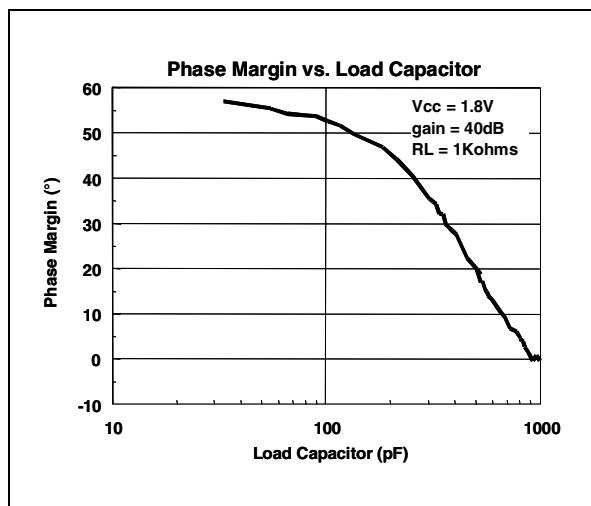


Figure 35 :

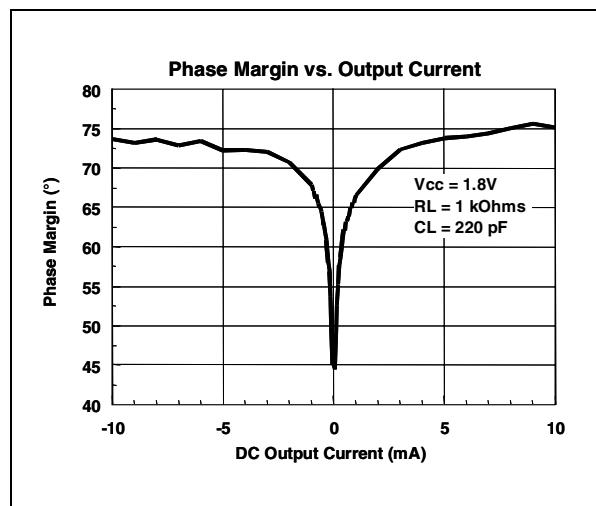


Figure 33 :

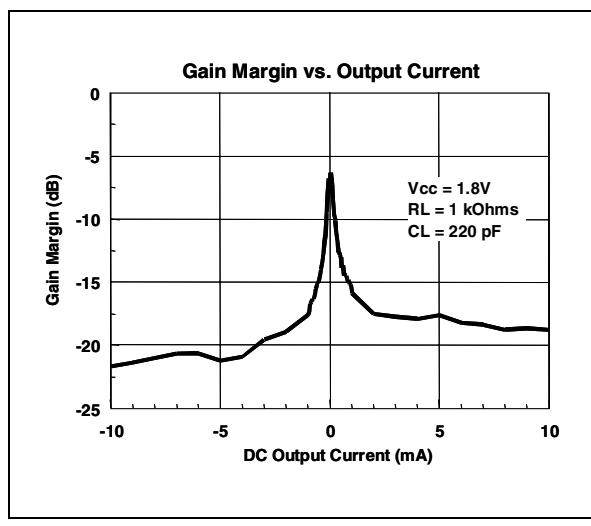


Figure 36 :

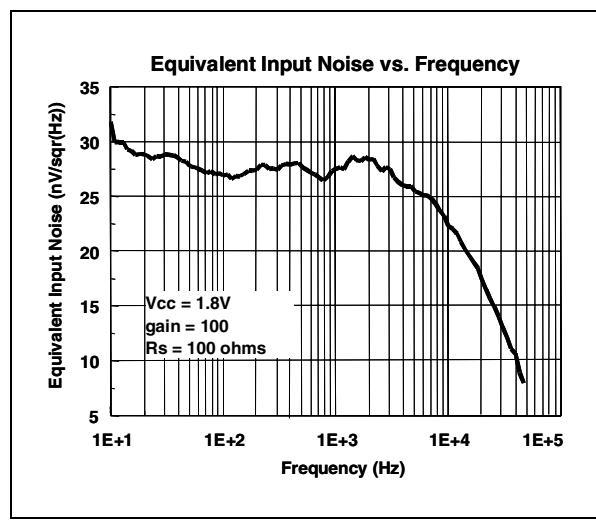


Figure 37 :

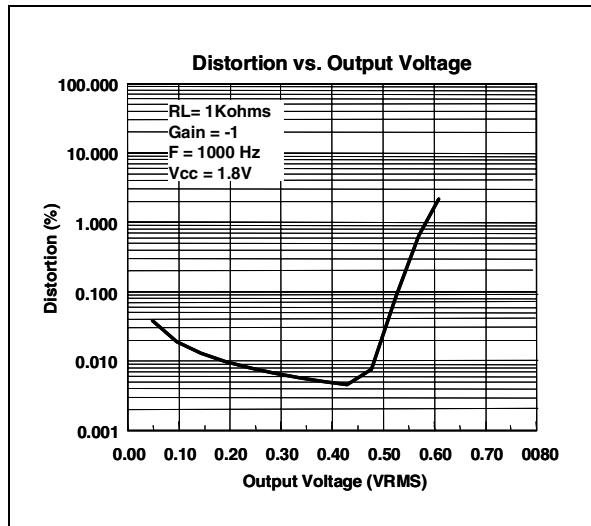


Figure 40 :

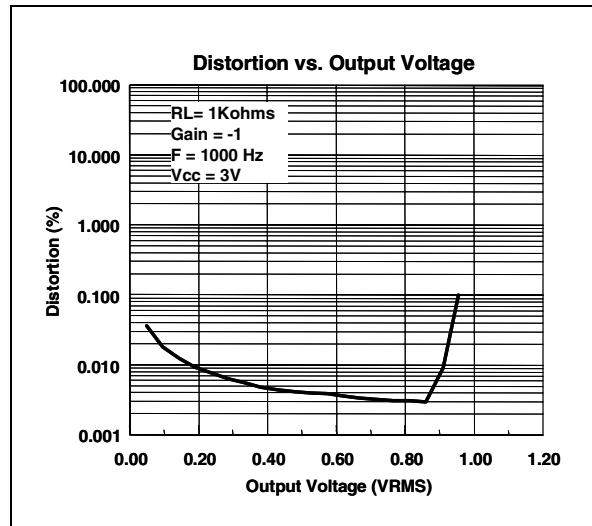


Figure 38 :

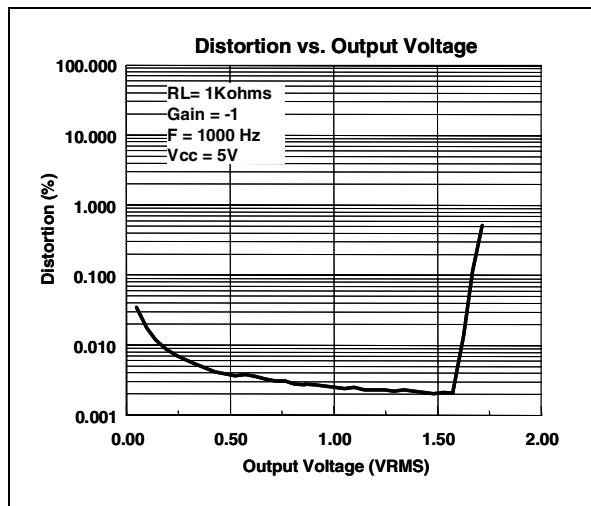


Figure 41 :

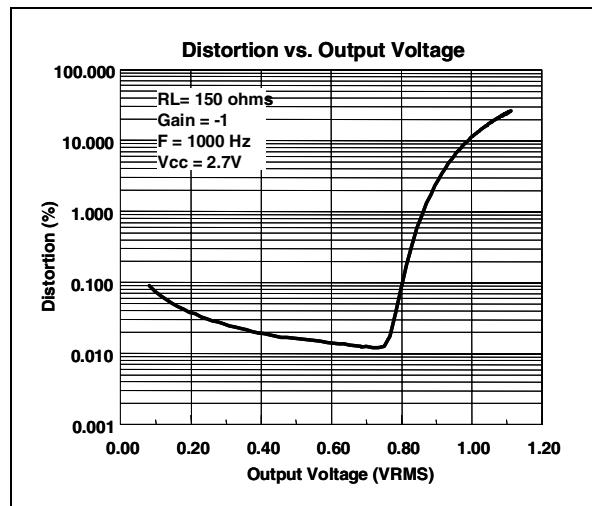


Figure 39 :

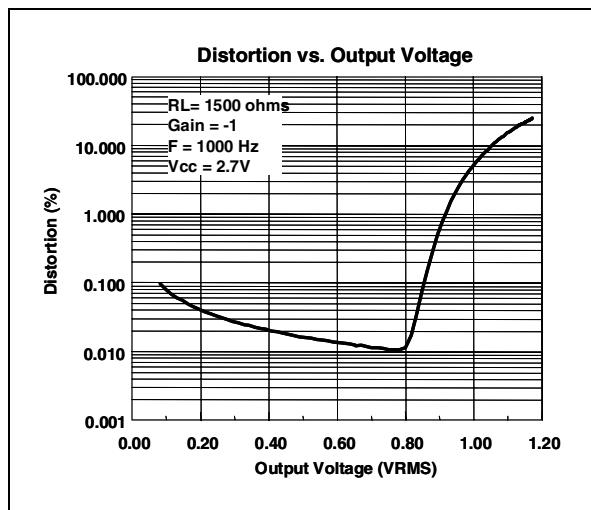


Figure 42 :

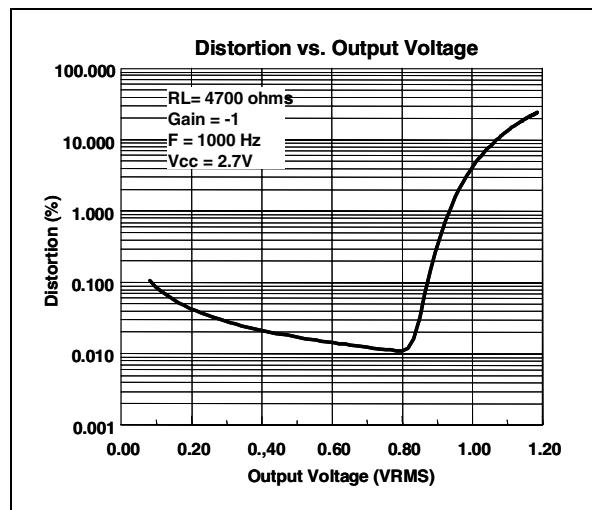


Figure 43 :

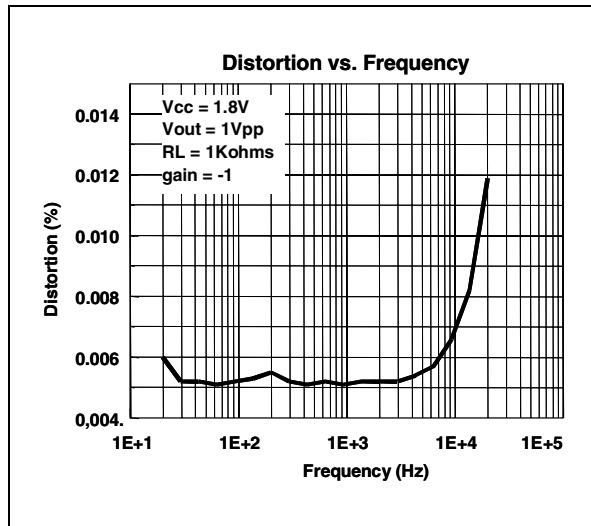


Figure 46 :

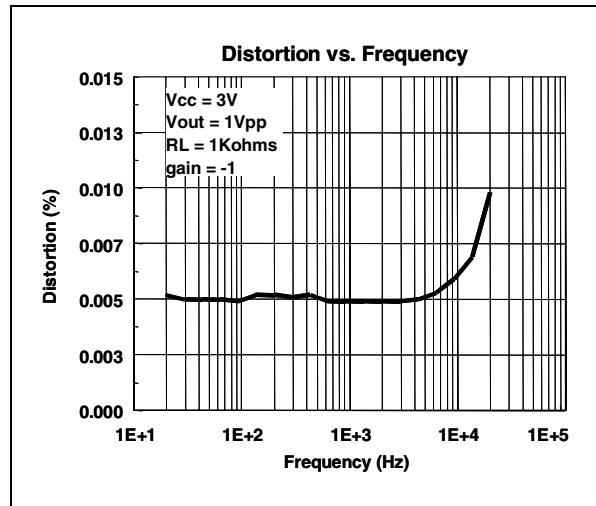


Figure 44 :

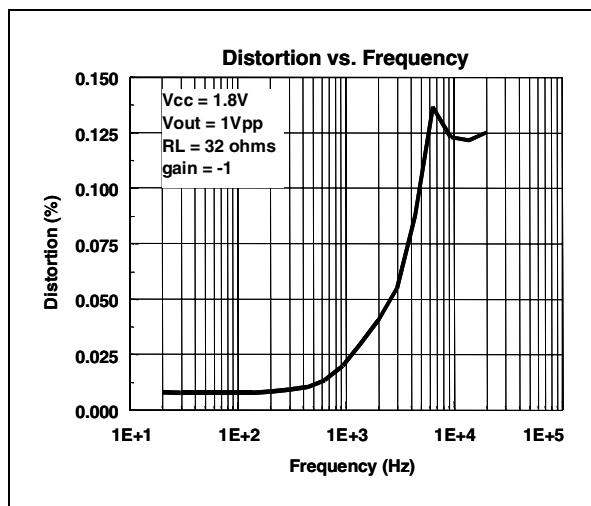


Figure 47 :

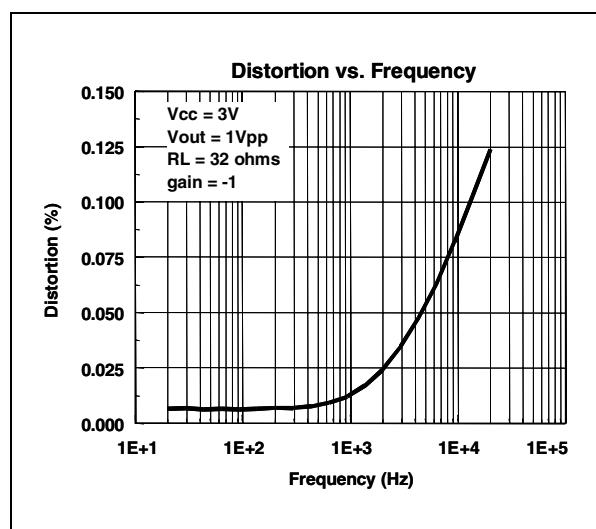
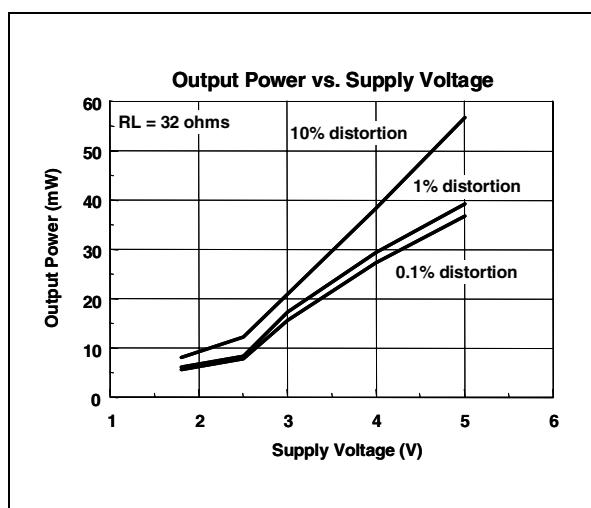


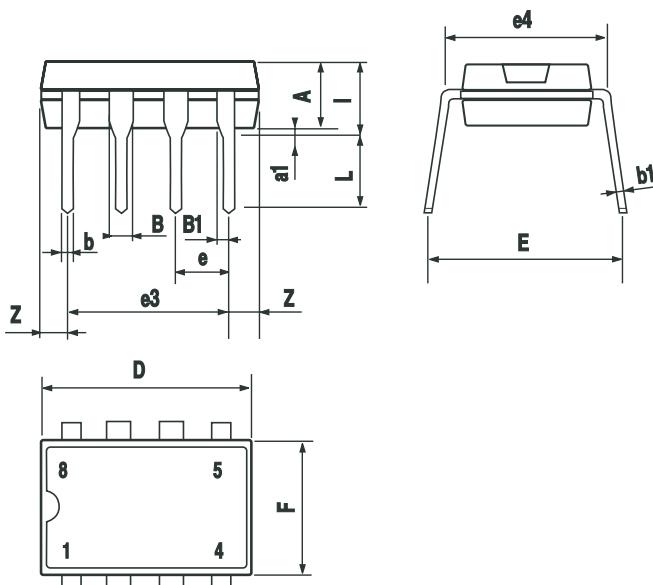
Figure 45 :



### 3 Package Mechanical Data

#### 3.1 DIP8 package

Plastic DIP-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

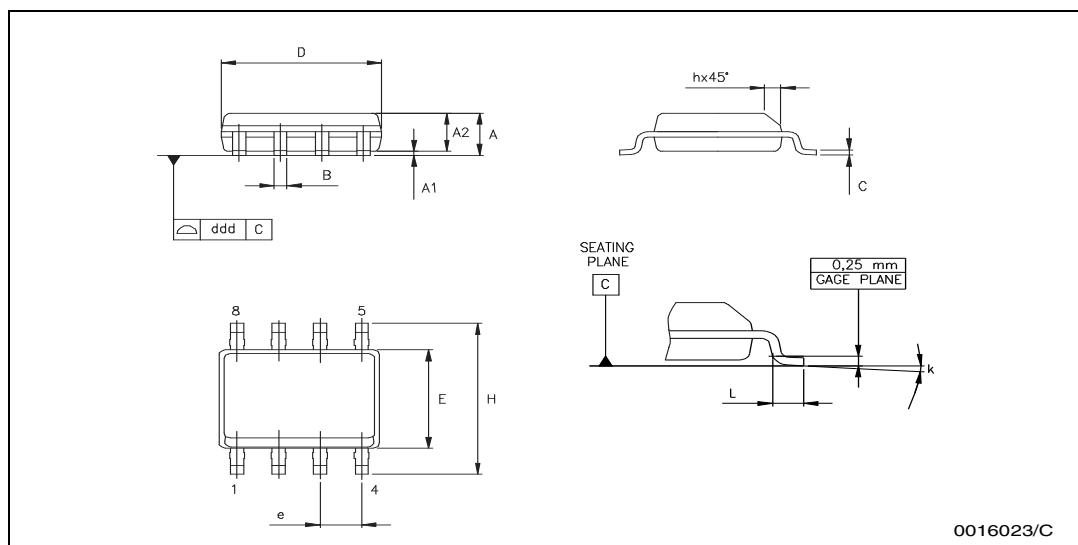
  


P001F

## 3.2 SO8 package

## SO-8 MECHANICAL DATA

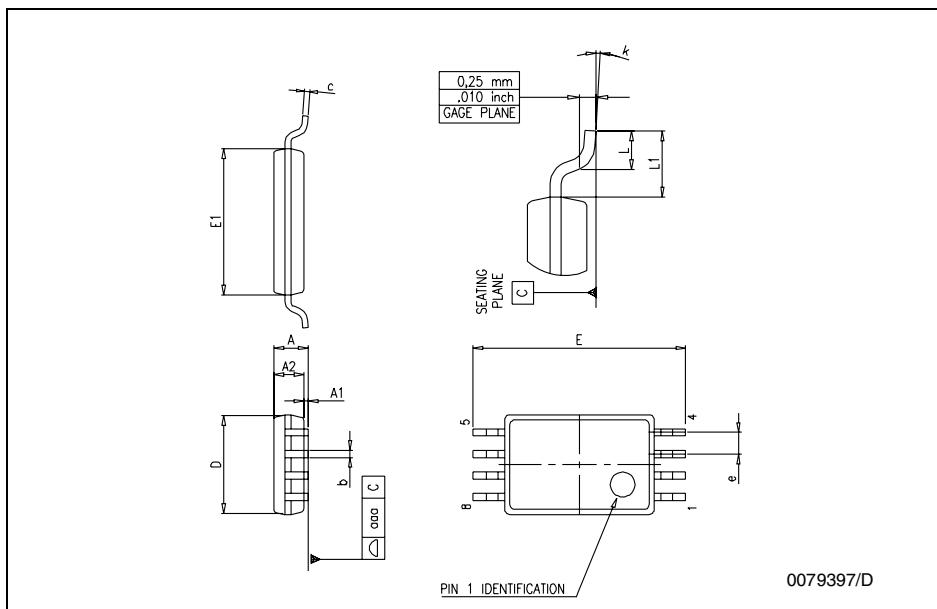
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



### 3.3 TSSOP8 package

**TSSOP8 MECHANICAL DATA**

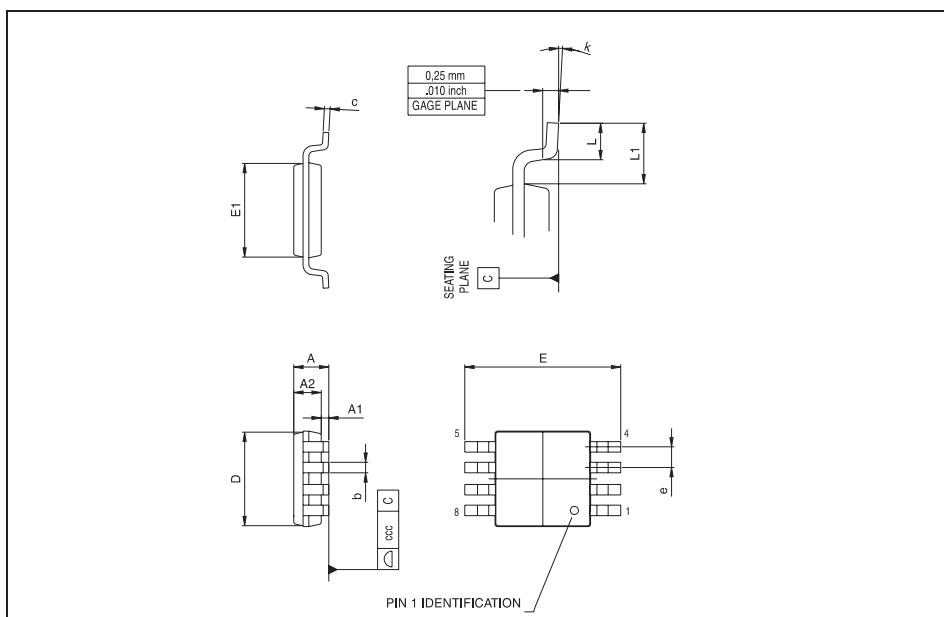
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	



### 3.4 Mini SO8 package

**miniSO-8 MECHANICAL DATA**

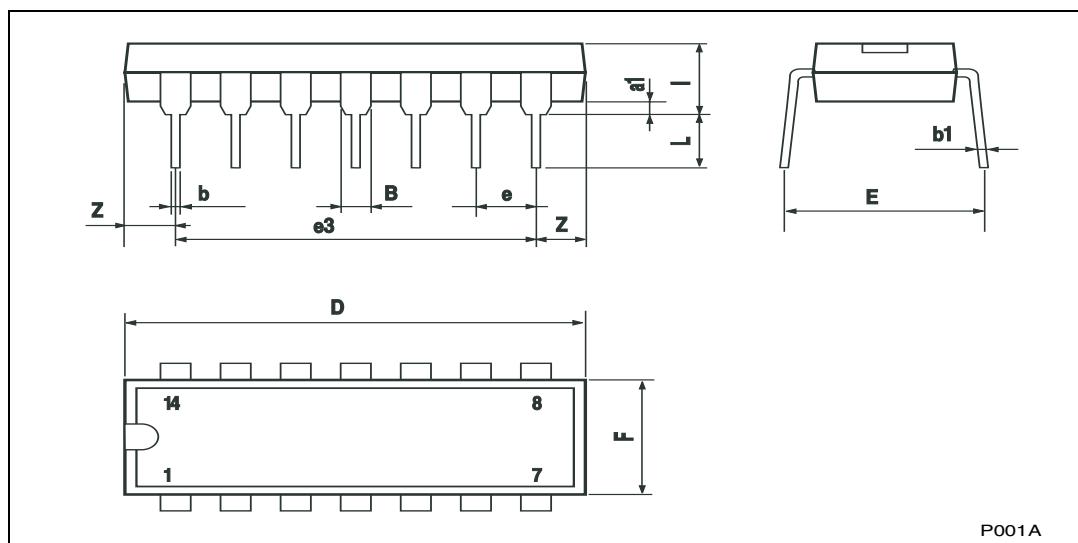
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



## 3.5 DIP14 package

Plastic DIP-14 MECHANICAL DATA

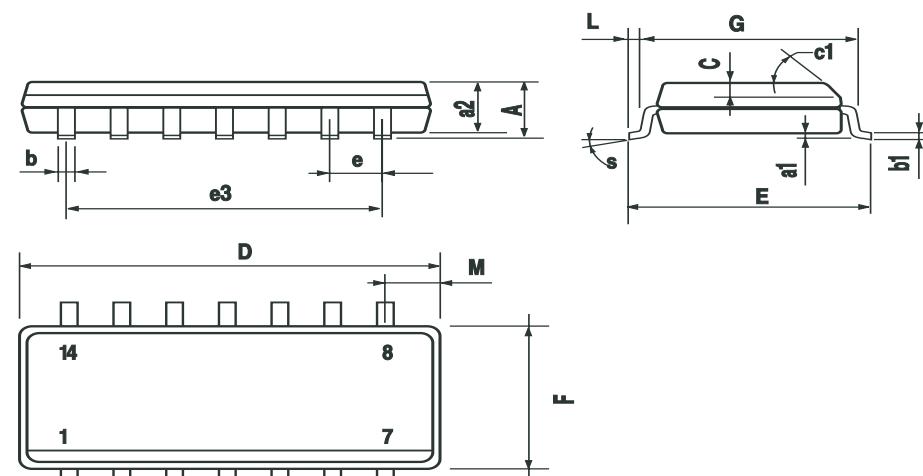
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

## 3.6 SO14 package

SO-14 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1			45° (typ.)			
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S			8° (max.)			

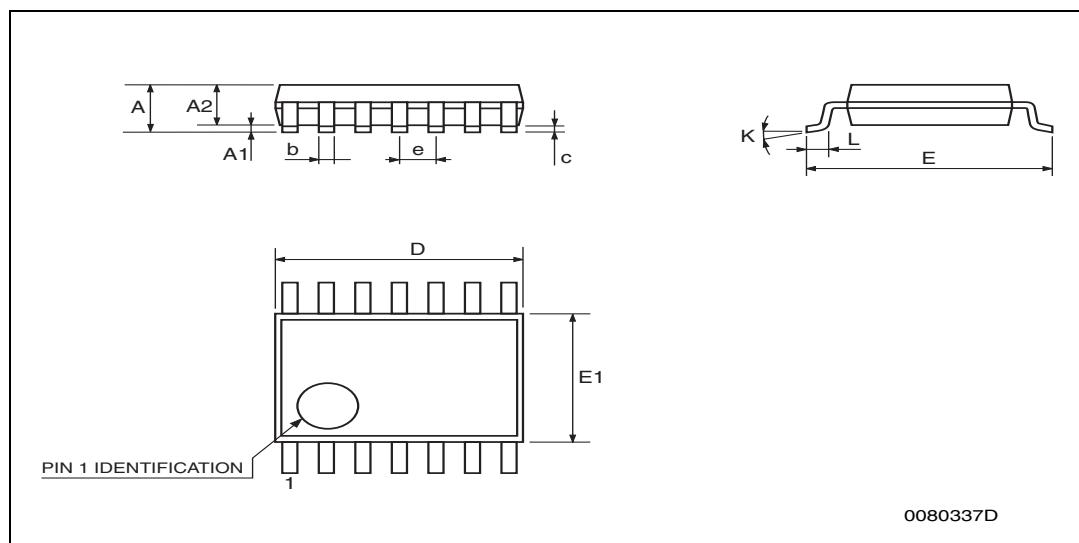
The mechanical drawings illustrate the physical dimensions of the SO-14 package. The top view shows the package body with pins numbered 1 through 14. The side view shows the profile with height dimensions L, G, and F. The cross-sectional view provides a detailed look at the lead structure with dimensions A, b, c, d, e, e3, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z, and z1. Specific callouts highlight features like the lead angle (c1) and lead thickness (b1).

PO13G

### 3.7 TSSOP14 package

**TSSOP14 MECHANICAL DATA**

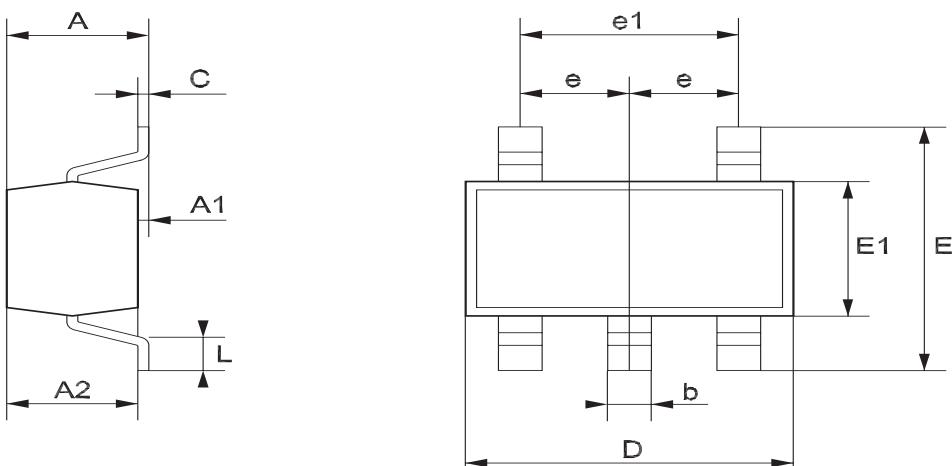
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



### 3.8 SOT23-5 package

**SOT23-5L MECHANICAL DATA**

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6



## 4 Revision History

Date	Revision	Description of Changes
01 April 2002	1	First Release
01 Jan. 2005	2	Modifications on AMR <i>Table 1 on page 2</i> (explanation of Vid and Vi limits)

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