

## Output Rail-to-Rail Very Low Noise Operational Amplifier

- Rail-to-rail output voltage swing  
 $\pm 2.4V @ V_{CC} = \pm 2.5V$
- Very low noise level:  $4nV/\sqrt{Hz}$
- Ultra low distortion: 0.003%
- High dynamic features: 12MHz,  $4V/\mu s$
- Operating range: 2.7V to 10V
- ESD protection (2kV)
- Latch-up immunity (class A)
- Available in:
  - SOT23-5
  - QFN8 (3x3) micropackage

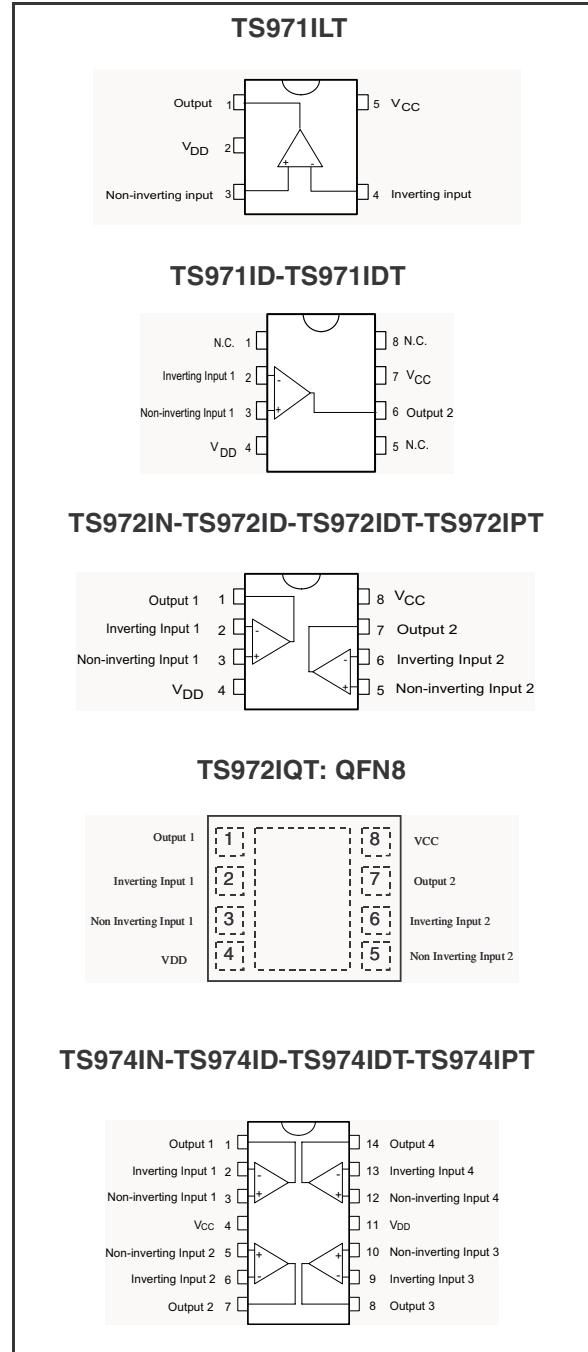
### Description

The TS97x family of operational amplifiers is able to operate with voltages as low as  $\pm 1.35V$  and featuring output rail-to-rail signal swing. The TS97x boasts characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio pre-amplification.

The TS971 is housed in the space-saving 5 pins SOT23 package which simplifies the board design because of the ability to be placed everywhere (outside dimensions are 2.8mm x 2.9mm).

### Applications

- Portable equipment (CD players, PDA)
- Portable communications (cell phones, pagers)
- Instrumentation & sensoring
- Professional audio circuits



# 1 Order Codes

Part Number	Temperature Range	Package	Packing	Marking	
TS971ID/IDT	-40°C, +125°C	SO-8	Tube or Tape & Reel	971I	
TS971ILT		SOT23-5L	Tape & Reel	K120	
TS971IYLT		SOT23-5L (automotive grade level)		K121	
TS971IYD/IYDT		SO-8 (automotive grade level)	Tube or Tape & Reel	971Y	
TS972IN		DIP8	Tube	TS972IN	
TS972ID/IDT		SO-8	Tube or Tape & Reel	972I	
TS972IPT		TSSOP8 (Thin Shrink Outline Package)	Tape & Reel		
TS972IQT		DFN8 (dual micro lead frame package)			
TS972IYD/IYDT		SO-8 (automotive grade level)	Tube or Tape & Reel	972Y	
TS972IYPT		TSSOP8 (automotive grade level)	Tape & Reel	972IY	
TS974IN		DIP14	Tube	TS974IN	
TS974ID/IDT		SO-14	Tube or Tape & Reel	974I	
TS974IPT		TSSOP14 (Thin Shrink Outline Package)	Tape & Reel		
TS974IYD/IYDT		SO-14 (automotive grade level)	974Y		
TS974IYPT		TSSOP14 (automotive grade level)	974IY		

## 2 Absolute Maximum Ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	12	V
$V_{id}$	Differential Input Voltage <sup>(2)</sup>	$\pm 1$	V
$V_{in}$	Input Voltage <sup>(3)</sup>	$V_{DD}-0.3$ to $V_{CC}+0.3$	V
$T_{oper}$	Operating Free Air Temperature Range	-40 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	
$T_j$	Maximum Junction Temperature	150	°C
$R_{thja}$	Thermal Resistance Junction to Ambient <sup>(4)</sup> SOT23-5 QFN8 SO8 SO14 TSSOP8 TSSOP14	250 50 125 103 120 100	°C/W
$R_{thjc}$	Thermal Resistance Junction to Case SOT23-5 QFN8 SO8 SO14 TSSOP8 TSSOP14	81 5.2 40 31 37 32	°C/W
ESD	HBM: Human Body Model <sup>(5)</sup>	2	kV
	MM: Machine Model <sup>(6)</sup>	200	V
	CDM: Charged Device Model	1.5	kV
	Lead Temperature (soldering, 10sec) <sup>(7)</sup>	260	°C

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed  $V_{CC} + 0.3V$ .
4. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
5. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
6. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.
7. No value specified for CDM on SOT23-5 package.

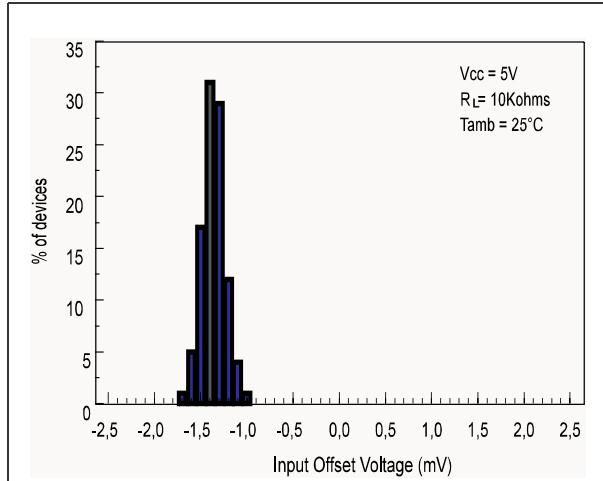
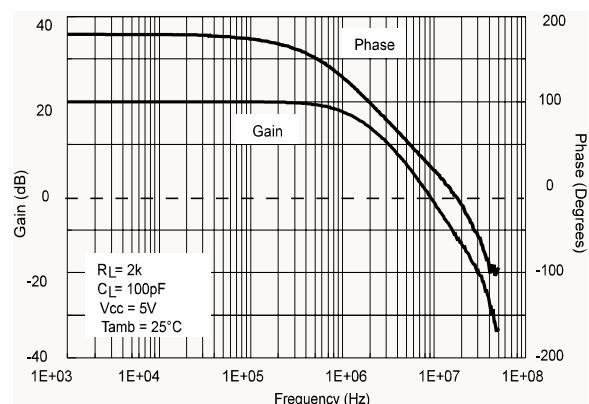
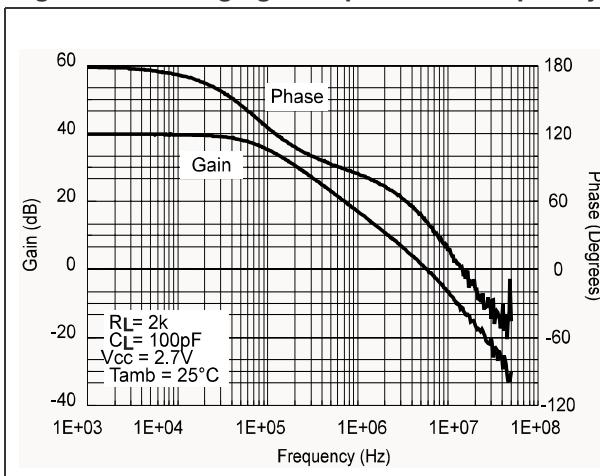
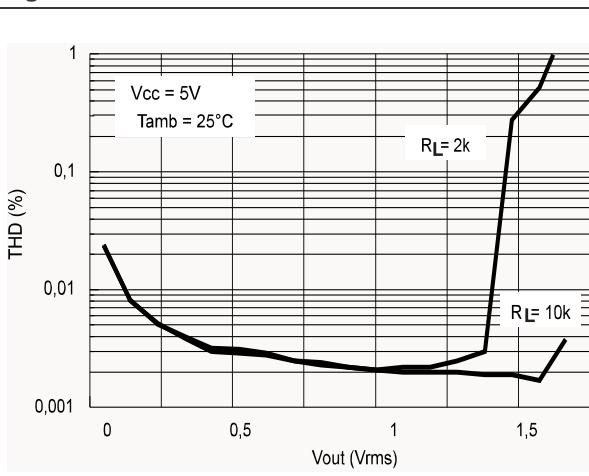
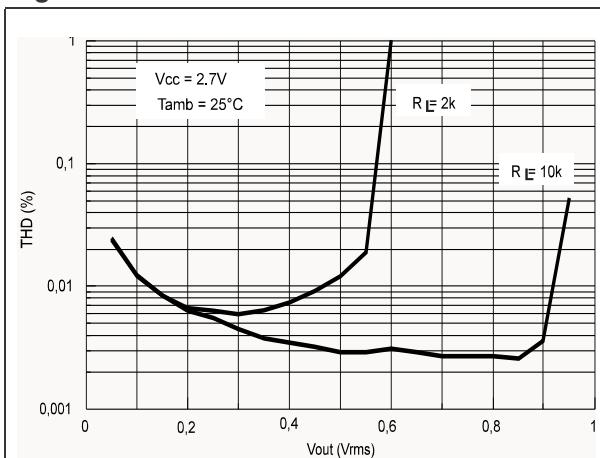
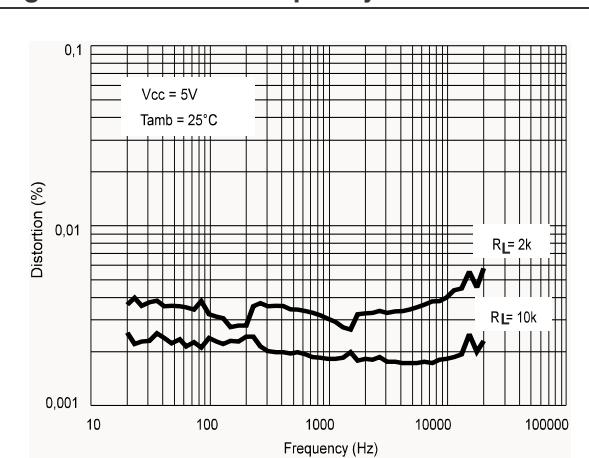
**Table 2. Operating conditions**

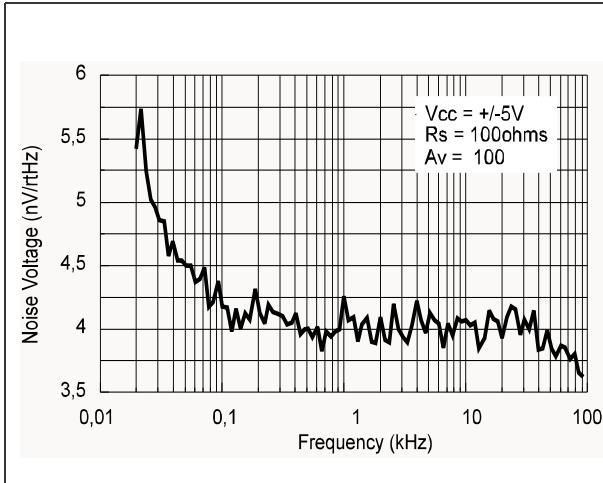
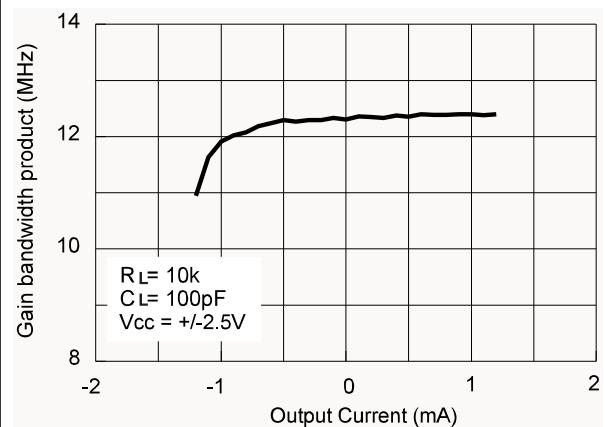
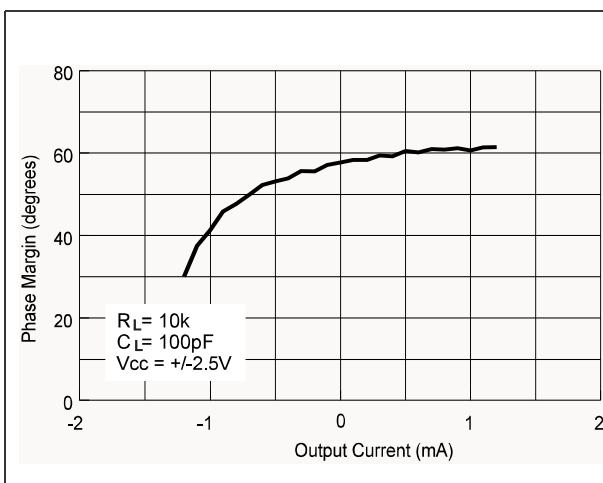
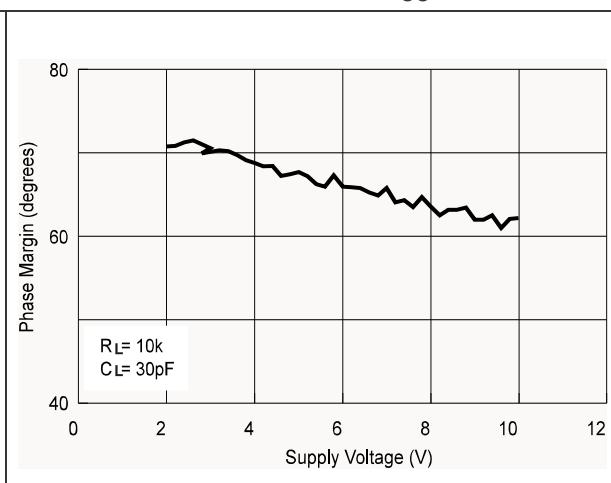
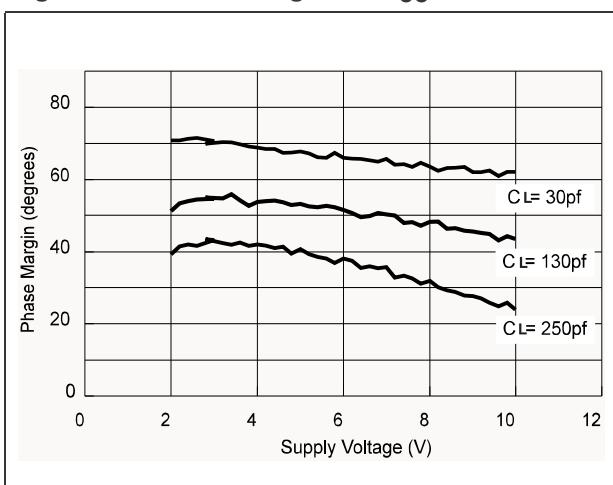
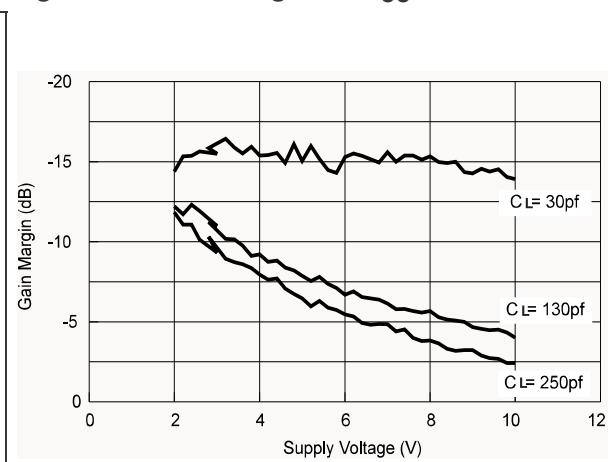
Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	2.7 to 10	V
$V_{icm}$	Common Mode Input Voltage Range	$V_{DD} +1.15$ to $V_{CC} -1.15$	V
$T_{oper}$	Operating Free Air Temperature Range	-40 to +125	°C

### 3 Electrical Characteristics

**Table 3.**  $V_{CC} = +2.5V$ ,  $V_{DD} = -2.5V$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage	$T_{min} \leq T_{amb} \leq T_{max}$		1 7	5 7	mV
$DV_{io}$	Input Offset Voltage Drift	$V_{icm} = 0V$ , $V_o = 0V$		5		$\mu V^\circ C$
$I_{io}$	Input Offset Current	$V_{icm} = 0V$ , $V_o = 0V$		10	150	nA
$I_{ib}$	Input Bias Current	$V_{icm} = 0V$ , $V_o = 0V$ $T_{min} \leq T_{amb} \leq T_{max}$		200 200	750 1000	nA
$V_{icm}$	Common Mode Input Voltage Range		-1.35		1.35	V
CMR	Common Mode Rejection Ratio	$V_{icm} = \pm 1.35V$	60	85		dB
SVR	Supply Voltage Rejection Ratio	$V_{CC} = \pm 2V$ to $\pm 3V$	60	70		dB
$A_{vd}$	Large Signal Voltage Gain	$R_L = 2k\Omega$	70	80		dB
$V_{OH}$	High Level Output Voltage	$R_L = 2k\Omega$	2	2.4		V
$V_{OL}$	Low Level Output Voltage	$R_L = 2k\Omega$		-2.4	-2	V
$I_{source}$	Output Source Current			1.5		mA
$I_{sink}$	Output Sink Current			100		mA
$I_{CC}$	Supply Current - per amplifier	Unity gain - No load		2	2.8	mA
GBP	Gain Bandwidth Product	$f = 100kHz$ , $R_L = 2k\Omega$ , $C_L = 100pF$	8.5	12		MHz
SR	Slew Rate	$A_V = 1$ , $V_{in} = \pm 1V$	2.8	4		V/ $\mu$ s
$\emptyset m$	Phase Margin at Unit Gain	$R_L = 2k\Omega$ , $C_L = 100pF$		60		Degrees
Gm	Gain Margin	$R_L = 2k\Omega$ , $C_L = 100pF$		10		dB
$e_n$	Equivalent Input Noise Voltage	$f = 100kHz$		4		nV/ $\sqrt{Hz}$
THD	Total Harmonic Distortion	$f = 1KHz$ , $A_V = -1$ , $R_L = 10k\Omega$		0.003		%

**Figure 1. Input offset voltage distribution****Figure 2. Voltage gain & phase vs. frequency****Figure 3. Voltage gain & phase vs. frequency****Figure 4. THS vs. Vout****Figure 5. THD vs. Vout****Figure 6. THD vs. frequency**

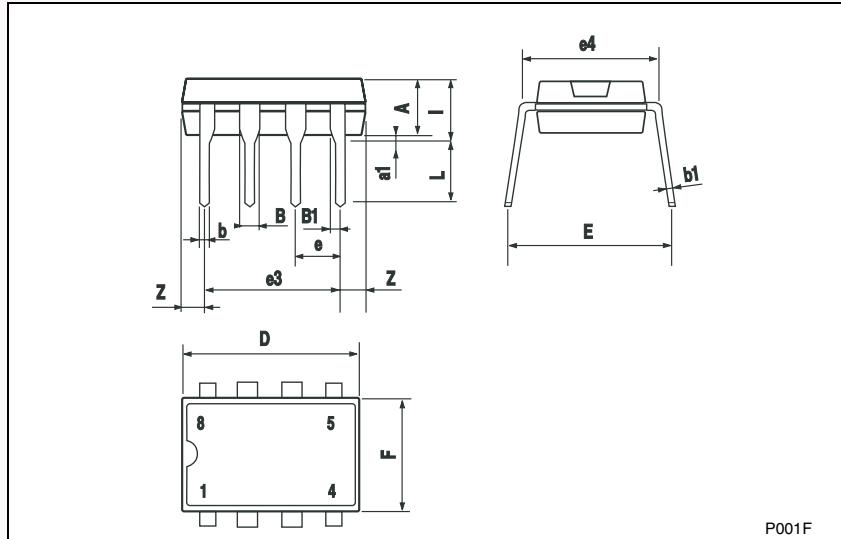
**Figure 7. Noise voltage vs. frequency****Figure 8. Gain bandwidth product vs. I<sub>out</sub>****Figure 9. Phase margin vs. I<sub>out</sub>****Figure 10. Phase margin vs. V<sub>CC</sub>****Figure 11. Phase margin vs. V<sub>CC</sub>****Figure 12. Gain margin vs. V<sub>CC</sub>**

## 4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 4.1 DIP8 Package

Plastic DIP-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

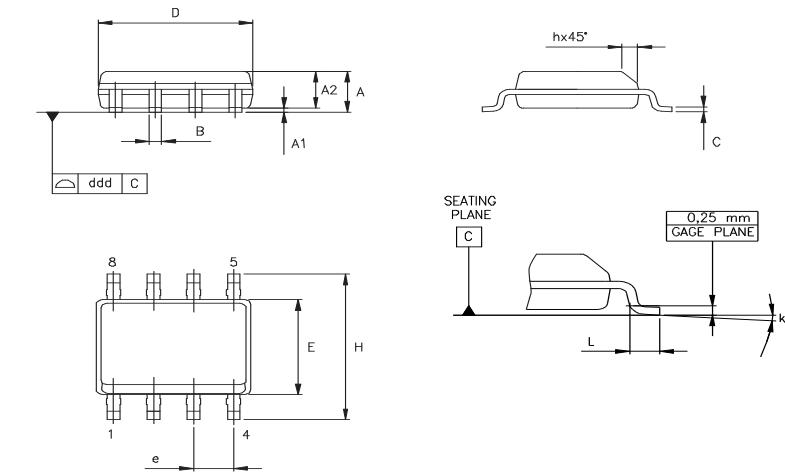
The technical drawing illustrates the Plastic DIP-8 package with three views: a top view showing the chip and pin layout with pins numbered 1 through 8, and two side views showing front and back dimensions. Dimensions are labeled as follows:

- Front View (Left):** Shows width **b**, height **Z**, lead thickness **a1**, lead pitch **B**, body width **B1**, and body height **e**.
- Side View (Top):** Shows total height **A**, lead thickness **a1**, lead pitch **B**, body width **B1**, body height **e**, and lead thickness **b1**.
- Side View (Bottom):** Shows total width **D**, lead thickness **b1**, and lead pitch **E**.
- Bottom View (Center):** Shows the chip and pin layout with pins numbered 1 through 8.

P001F

## 4.2 SO-8 Package

SO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04

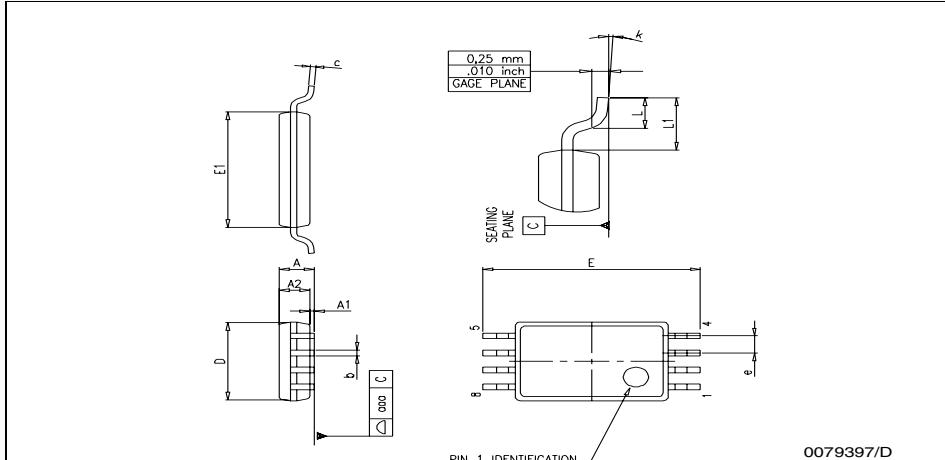
  


The technical drawings illustrate the physical dimensions of the SO-8 package. The top view shows the footprint with pins numbered 1 through 8. The side view shows height H and lead angle hx45°. The cross-sectional view shows the thickness of the package body, the seating plane, and the gage plane at 0.25 mm. Dimensions A through k are indicated in both millimeters and inches as defined in the table above.

0016023/C

### 4.3 TSSOP8 Package

TSSOP8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	

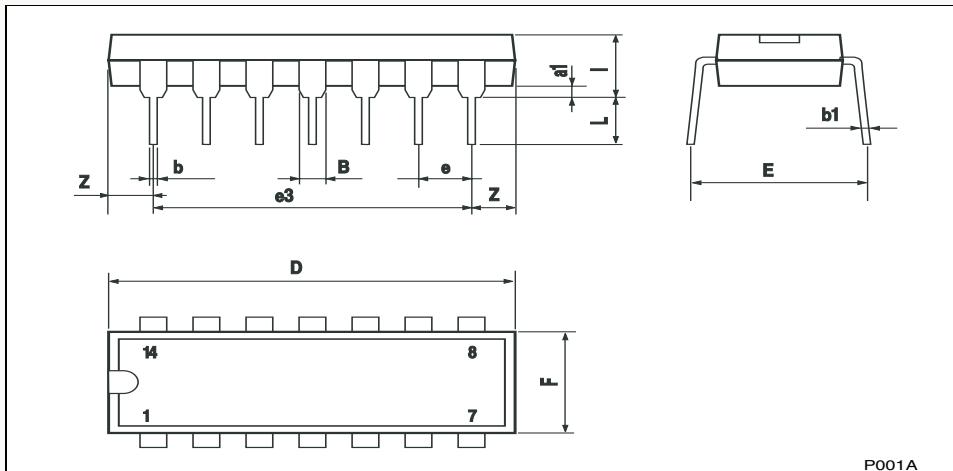
  


The technical drawing illustrates the physical dimensions of the TSSOP8 package. It includes a top view showing the chip size (E) and lead spacing (L), a side view showing height (A), lead thickness (A1), and lead width (A2), and a cross-sectional view showing lead height (b), lead thickness (c), lead pitch (D), lead width (E), lead height (F), lead thickness (G), and lead width (H). A note specifies a gage plane at 0.25 mm (0.010 inch). Pin 1 identification is also indicated.

0079397/D

## 4.4 DIP14 Package

Plastic DIP-14 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

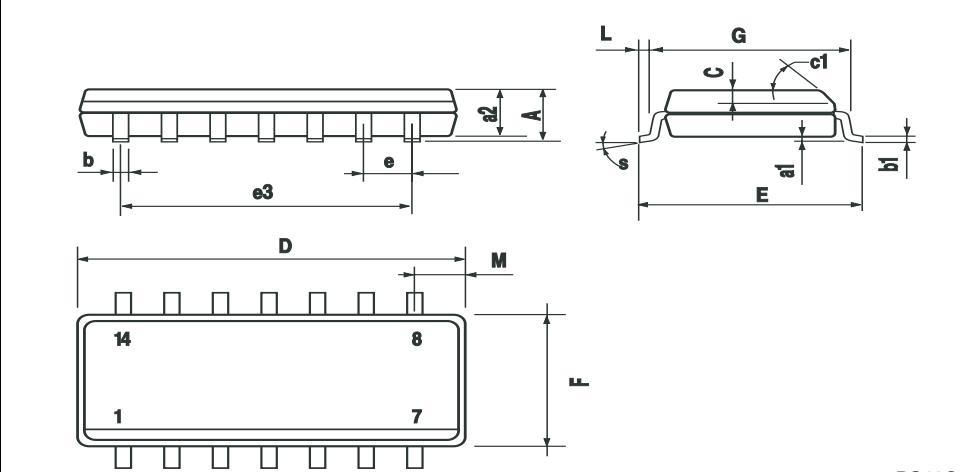
  


The technical drawings illustrate the mechanical dimensions of a Plastic DIP-14 package. The top view shows the footprint with pins numbered 1 through 14. Key dimensions labeled are: a1 (pin height), B (total width), b (width of one pin), b1 (width of one lead), e (pin pitch), e3 (lead length), F (lead thickness), I (lead height), L (lead width), and Z (lead thickness). The side view provides a profile of the package, showing its height (a1) and the lead profile with dimensions b1 and E.

P001A

## 4.5 SO-14 Package

SO-14 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a <sub>1</sub>	0.1		0.2	0.003		0.007
a <sub>2</sub>			1.65			0.064
b	0.35		0.46	0.013		0.018
b <sub>1</sub>	0.19		0.25	0.007		0.010
C		0.5			0.019	
c <sub>1</sub>			45° (typ.)			
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e <sub>3</sub>		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S			8° (max.)			

The diagram illustrates the SO-14 package with three views: a top view showing the lead configuration with lead numbers 1 through 14, a side view showing the profile and lead spacing, and a bottom view showing the lead spacing and overall width. Dimensions labeled include A, a1, a2, b, b1, C, c1, D, e, e3, F, G, L, M, and S.

PO13G

## 4.6 TSSOP14 Package

TSSOP14 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

The technical drawings illustrate the physical dimensions of the TSSOP14 package. The top view shows the overall width (D), height (E1), and lead spacing (L). A separate diagram shows the lead profile with lead thickness (K) and lead spacing (L). Pin 1 identification is indicated by a circle at the bottom left corner of the chip area.

0080337D

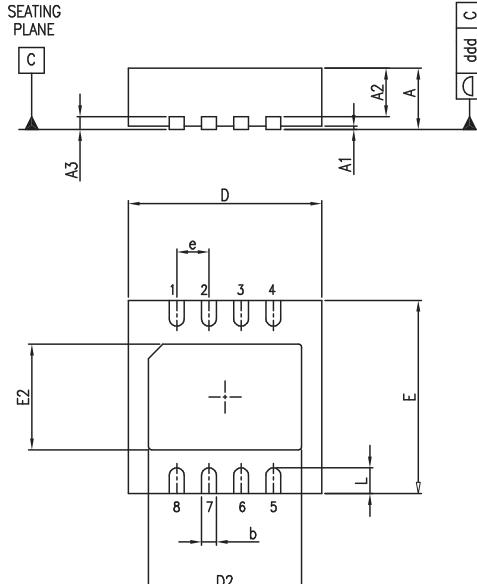
## 4.7 SOT23-5 Package

SOT23-5L MECHANICAL DATA						
DIM.	mm.			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6

The diagram illustrates the SOT23-5 package with two views. The left view shows the front profile with dimensions A (total height), C (lead thickness), A1 (lead gap), A2 (lead width), and L (lead length). The right view shows the top plan view with dimensions e1 (total width), e (lead pitch), b (lead thickness), D (total length), E (total height), and E1 (lead gap).

## 4.8 DFN8 Package

DFN8 (3x3) MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.5	35.4	39.4
A1		0.02	0.05		0.8	2.0
A2		0.70			27.6	
A3		0.20			7.9	
b	0.18	0.23	0.30	7.1	9.1	11.8
D	2.875	3.00	3.125		118.1	
D2	2.23	2.38	2.48	87.8	93.7	97.7
E	2.875	3.00	3.125		118.1	
E2	1.49	1.64	1.74	58.7	64.6	68.5
e		0.50			19.7	
L	0.30	0.40	0.50	11.8	15.7	19.7

The diagram illustrates the physical dimensions of the DFN8 package. The top view shows the overall package size (D x E), lead pitch (A2), lead thickness (e), lead height (A3), and lead width (b). The cross-section provides a detailed look at the internal structure, including the seating plane (C), lead thickness (e), bond pads (numbered 1 through 8), and the lead profile (D2).

## 5 Revision history

Date	Revision	Changes
Nov. 2002	1	First Release
May 2005	2	Modifications on AMR <i>Table 1 on page 3</i> (explanation of Vid and Vi limits)
Aug. 2005	3	PPAP references inserted in the datasheet see <i>Table 1 on page 2</i> .
Dec. 2005	4	<ul style="list-style-type: none"> <li>– Thermal Resistance Junction to Case data added in <i>Table 1. on page 3</i></li> <li>– Missing PPAP references inserted in the datasheet see <i>Table 1 on page 2</i>.</li> </ul>

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.  
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)