



BTA12, BTB12 and T12 Series

SNUBBERLESS™, LOGIC LEVEL & STANDARD

12A TRIACs

Table 1: Main Features

Symbol	Value	Unit
$I_{T(RMS)}$	12	A
V_{DRM}/V_{RRM}	600 and 800	V
$I_{GT}(Q_1)$	5 to 50	mA

DESCRIPTION

Available either in through-hole or surface-mount packages, the **BTA12**, **BTB12** and **T12** triac series is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control operation in light dimmers, motor speed controllers,...

The snubberless versions (BTA/BTB...W and T12 series) are specially recommended for use on inductive loads, thanks to their high commutation performances.

Logic level versions are designed to interface directly with low power drivers such as microcontrollers.

By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at $2500V_{RMS}$) complying with UL standards (File ref.: E81734).

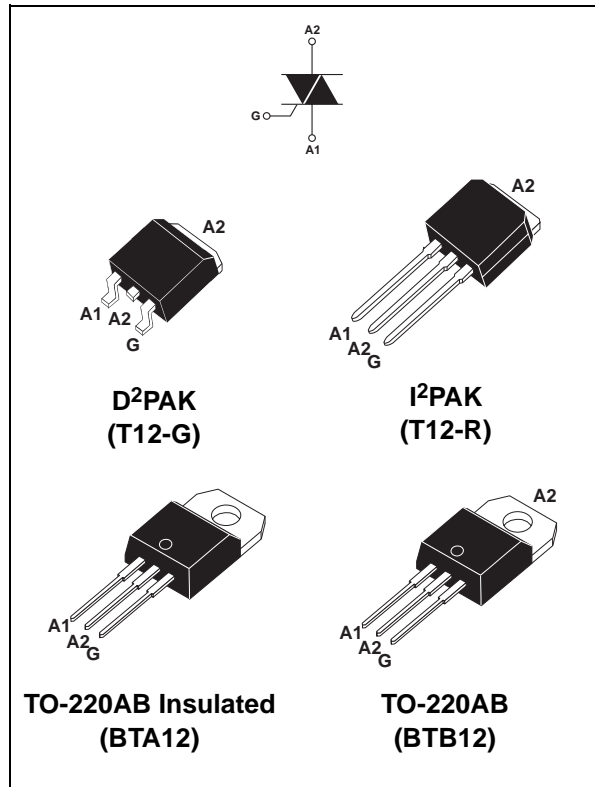


Table 2: Order Codes

Part Number	Marking
BTA12-xxxxxRG	See page table 8 on page 9
BTB12-xxxxxRG	
T12xx-xxxG	
T12xx-xxxG-TR	
T12xx-xxxR	

BTA12, BTB12 and T12 Series

Table 3: Absolute Maximum Ratings

Symbol	Parameter		Value	Unit	
$I_{T(RMS)}$	RMS on-state current (full sine wave)	I ² PAK/D ² PAK/ TO-220AB	$T_c = 105^\circ\text{C}$	12	A
		TO-220AB Ins.	$T_c = 90^\circ\text{C}$		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	F = 50 Hz	t = 20 ms	120	A
		F = 60 Hz	t = 16.7 ms	126	
I^2t	I^2t Value for fusing	$t_p = 10$ ms		78	A ² s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100$ ns	F = 120 Hz	$T_j = 125^\circ\text{C}$	50	A/ μs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	$t_p = 10$ ms	$T_j = 25^\circ\text{C}$	$V_{DRM}/V_{RRM} + 100$	V
I_{GM}	Peak gate current	$t_p = 20$ μs	$T_j = 125^\circ\text{C}$	4	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ\text{C}$	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	$^\circ\text{C}$

Tables 4: Electrical Characteristics ($T_j = 25^\circ\text{C}$, unless otherwise specified)

■ **SNUBBERLESS and Logic Level (3 quadrants)**

Symbol	Test Conditions	Quadrant		T12		BTA12 / BTB12				Unit
				T1205	T1235	TW	SW	CW	BW	
I_{GT} (1)	$V_D = 12$ V $R_L = 30$ Ω	I - II - III	MAX.	5	35	5	10	35	50	mA
V_{GT}		I - II - III	MAX.	1.3						V
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3$ k Ω $T_j = 125^\circ\text{C}$	I - II - III	MIN.	0.2						V
I_H (2)	$I_T = 100$ mA		MAX.	10	35	10	15	35	50	mA
I_L	$I_G = 1.2$ I_{GT}	I - III	MAX.	10	50	10	25	50	70	mA
		II		15	60	15	30	60	80	
dV/dt (2)	$V_D = 67\%$ V_{DRM} gate open $T_j = 125^\circ\text{C}$		MIN.	20	500	20	40	500	1000	V/ μs
(di/dt)c (2)	$(dV/dt)c = 0.1$ V/ μs $T_j = 125^\circ\text{C}$		MIN.	3.5		3.5	6.5			A/ms
	$(dV/dt)c = 10$ V/ μs $T_j = 125^\circ\text{C}$			1		1	2.9			
	Without snubber $T_j = 125^\circ\text{C}$				6.5			6.5	12	

■ Standard (4 quadrants)

Symbol	Test Conditions	Quadrant		BTA12 / BTB12		Unit
				C	B	
I_{GT} (1)	$V_D = 12\text{ V}$ $R_L = 30\ \Omega$	I - II - III IV	MAX.	25 50	50 100	mA
V_{GT}		ALL	MAX.	1.3		V
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3\text{ k}\Omega$ $T_j = 125^\circ\text{C}$	ALL	MIN.	0.2		V
I_H (2)	$I_T = 500\text{ mA}$		MAX.	25	50	mA
I_L	$I_G = 1.2 I_{GT}$	I - III - IV	MAX.	40	50	mA
		II		80	100	
dV/dt (2)	$V_D = 67\% V_{DRM}$ gate open $T_j = 125^\circ\text{C}$		MIN.	200	400	V/ μs
(dV/dt) _c (2)	$(di/dt)_c = 5.3\text{ A/ms}$ $T_j = 125^\circ\text{C}$		MIN.	5	10	V/ μs

Table 5: Static Characteristics

Symbol	Test Conditions			Value	Unit	
V_T (2)	$I_{TM} = 17\text{ A}$	$t_p = 380\ \mu\text{s}$	$T_j = 25^\circ\text{C}$	MAX.	1.55	V
V_{t0} (2)	Threshold voltage		$T_j = 125^\circ\text{C}$	MAX.	0.85	V
R_d (2)	Dynamic resistance		$T_j = 125^\circ\text{C}$	MAX.	35	m Ω
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$		$T_j = 25^\circ\text{C}$	MAX.	5	μA
			$T_j = 125^\circ\text{C}$		1	mA

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1.

Table 6: Thermal resistance

Symbol	Parameter		Value	Unit	
$R_{th(j-c)}$	Junction to case (AC)		I ² PAK / D ² PAK / TO-220AB	1.4	$^\circ\text{C/W}$
			TO-220AB Insulated	2.3	
$R_{th(j-a)}$	Junction to ambient	S = 1 cm ²	D ² PAK	45	$^\circ\text{C/W}$
			TO-220AB / I ² PAK TO-220AB Insulated	60	

S = Copper surface under tab.

Figure 1: Maximum power dissipation versus RMS on-state current (full cycle)

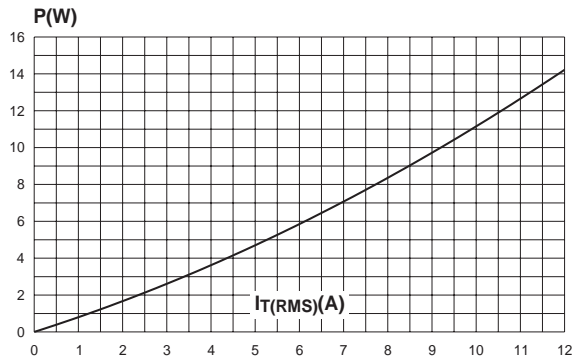


Figure 2: RMS on-state current versus case temperature (full cycle)

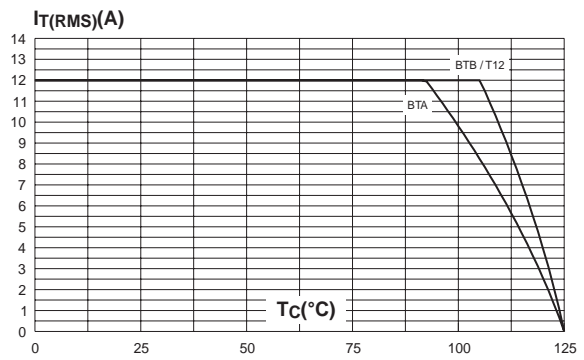


Figure 3: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm) (full cycle)

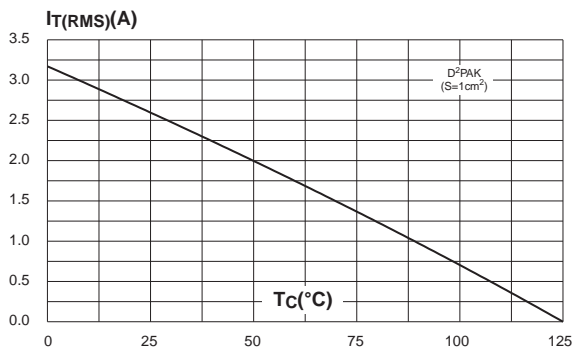


Figure 4: Relative variation of thermal impedance versus pulse duration

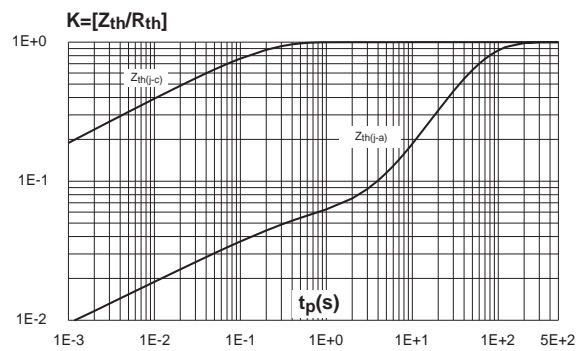


Figure 5: On-state characteristics (maximum values)

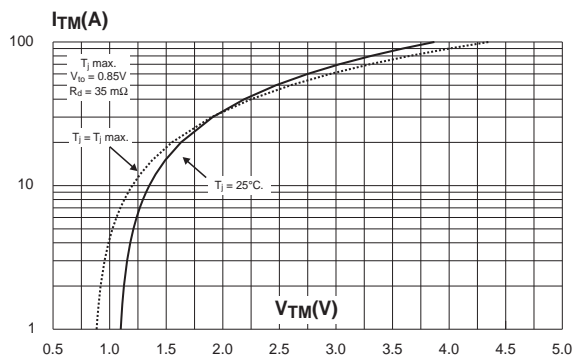


Figure 6: Surge peak on-state current versus number of cycles

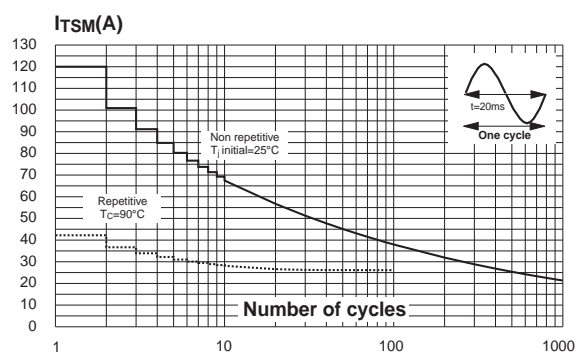


Figure 7: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms and corresponding value of I^2t

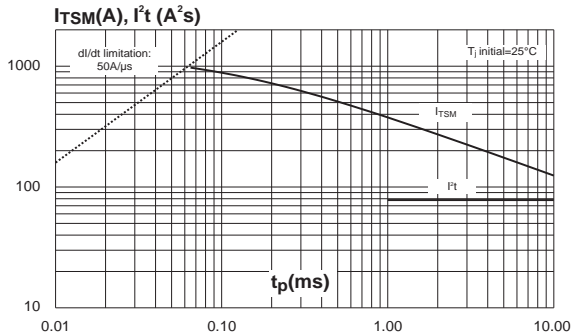


Figure 8: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

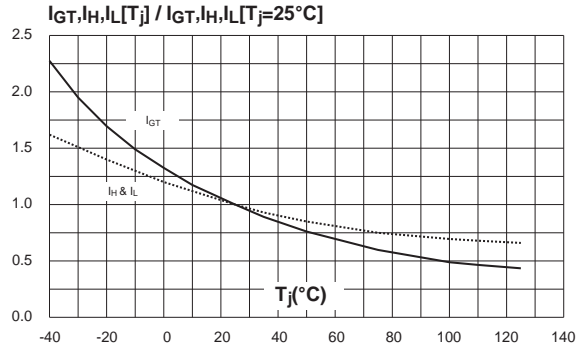


Figure 9: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values) (BW/CW/T1235)

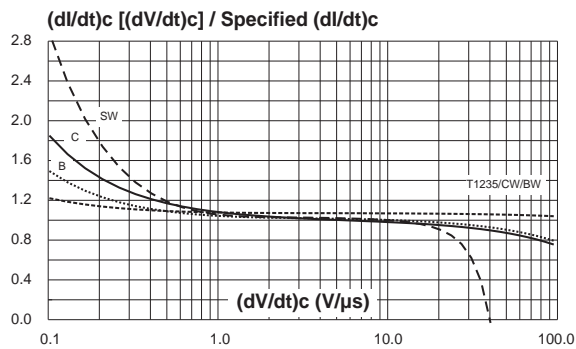


Figure 10: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values) (TW/T1205)

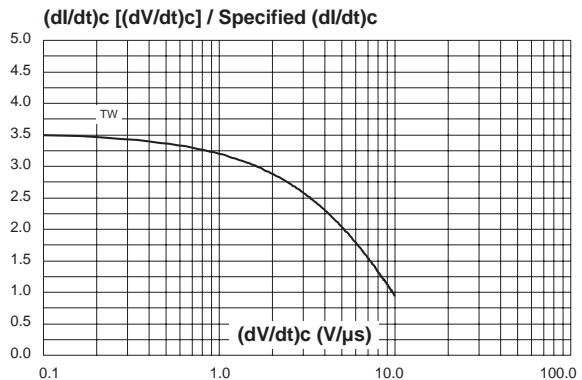


Figure 11: Relative variation of critical rate of decrease of main current versus junction temperature

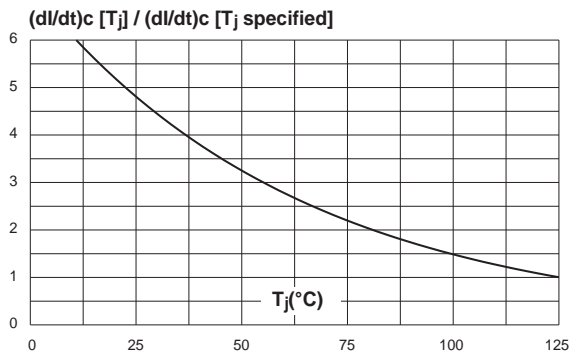
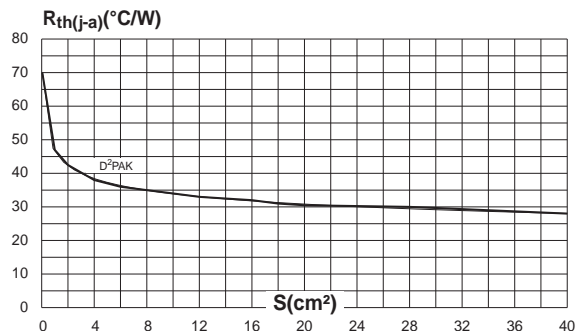


Figure 12: D²PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 μ m)



BTA12, BTB12 and T12 Series

Figure 13: Ordering Information Scheme (BTA and BTB series)

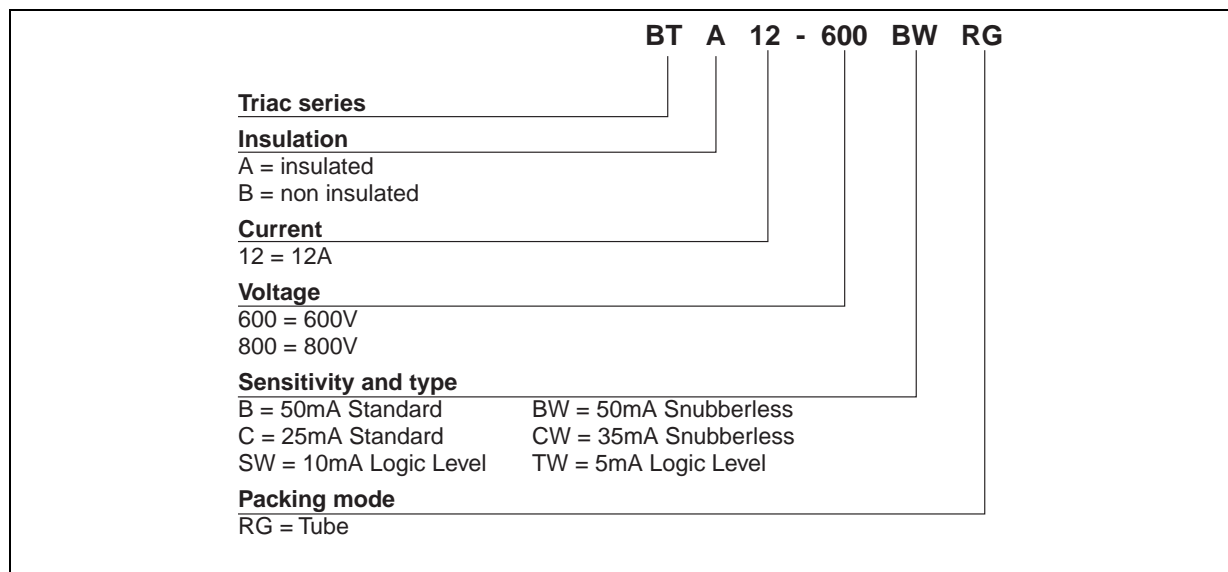


Figure 14: Ordering Information Scheme (T12 series)

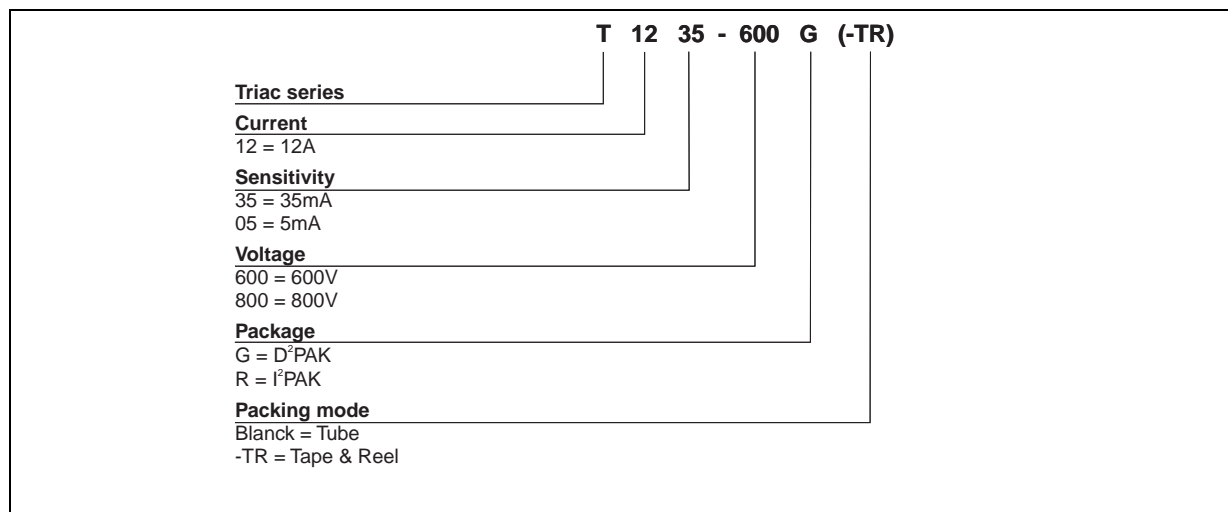


Table 7: Product Selector

Part Number	Voltage (xxx)		Sensitivity	Type	Package
	600 V	800 V			
BTA/BTB12-xxxBRG	X	X	50 mA	Standard	TO-220AB
BTA/BTB12-xxxBWRG	X	X	50 mA	Snubberless	TO-220AB
BTA/BTB12-xxxCRG	X	X	25 mA	Standard	TO-220AB
BTA/BTB12-xxxCWRG	X	X	35 mA	Snubberless	TO-220AB
BTA/BTB12-xxxSWRG	X	X	10 mA	Logic Level	TO-220AB
BTA/BTB12-xxxTWRG	X	X	5 mA	Logic Level	TO-220AB
T1205-xxxG	X	X	5 mA	Snubberless	D ² PAK
T1235-xxxG	X	X	35 mA	Snubberless	D ² PAK
T1235-xxxR	X	X	35 mA	Snubberless	I ² PAK

BTB: non insulated TO-220AB package

Figure 15: D²PAK Package Mechanical Data

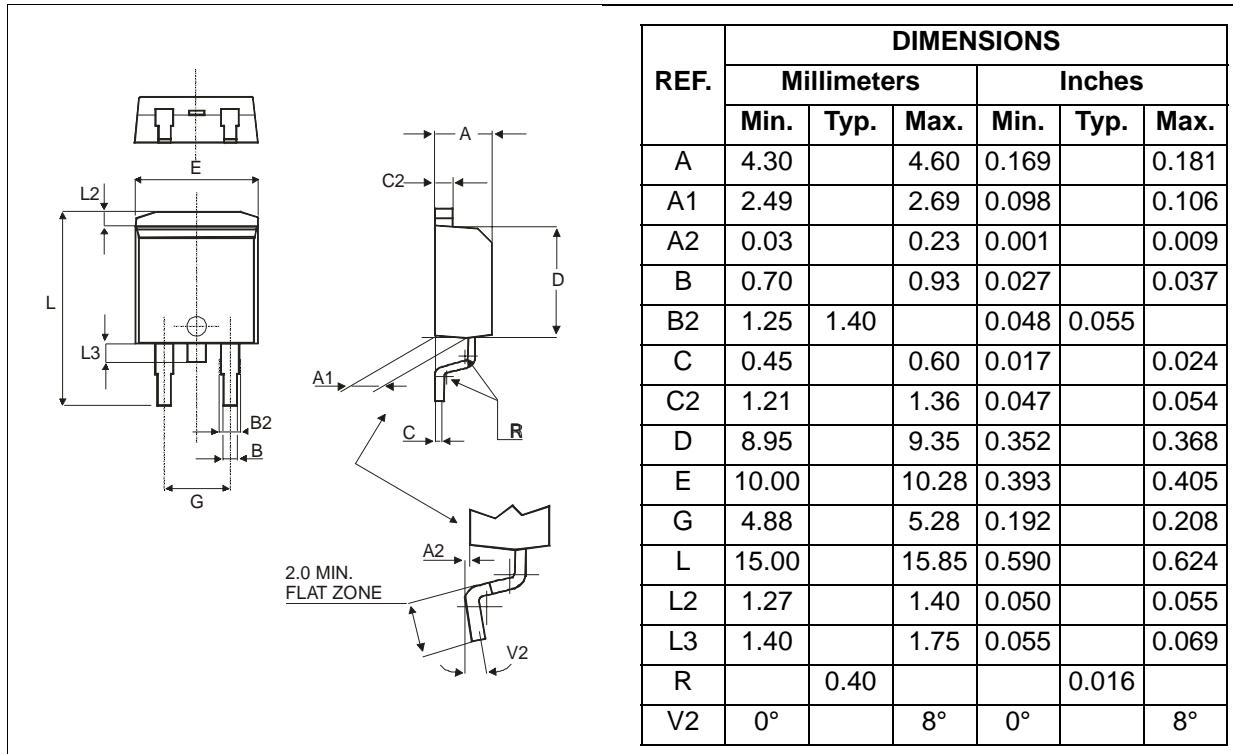
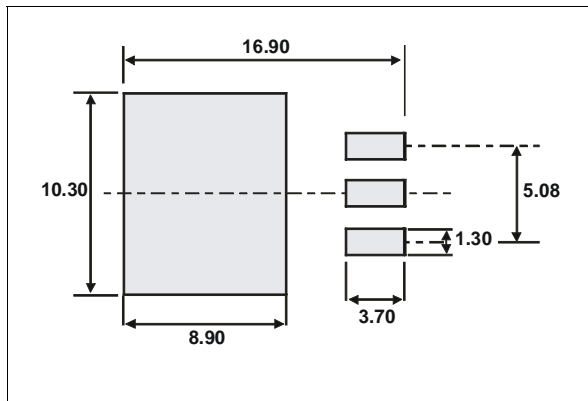


Figure 16: D²PAK Foot Print Dimensions (in millimeters)



BTA12, BTB12 and T12 Series

Figure 17: TO-220AB Insulated and non insulated) Package Mechanical Data

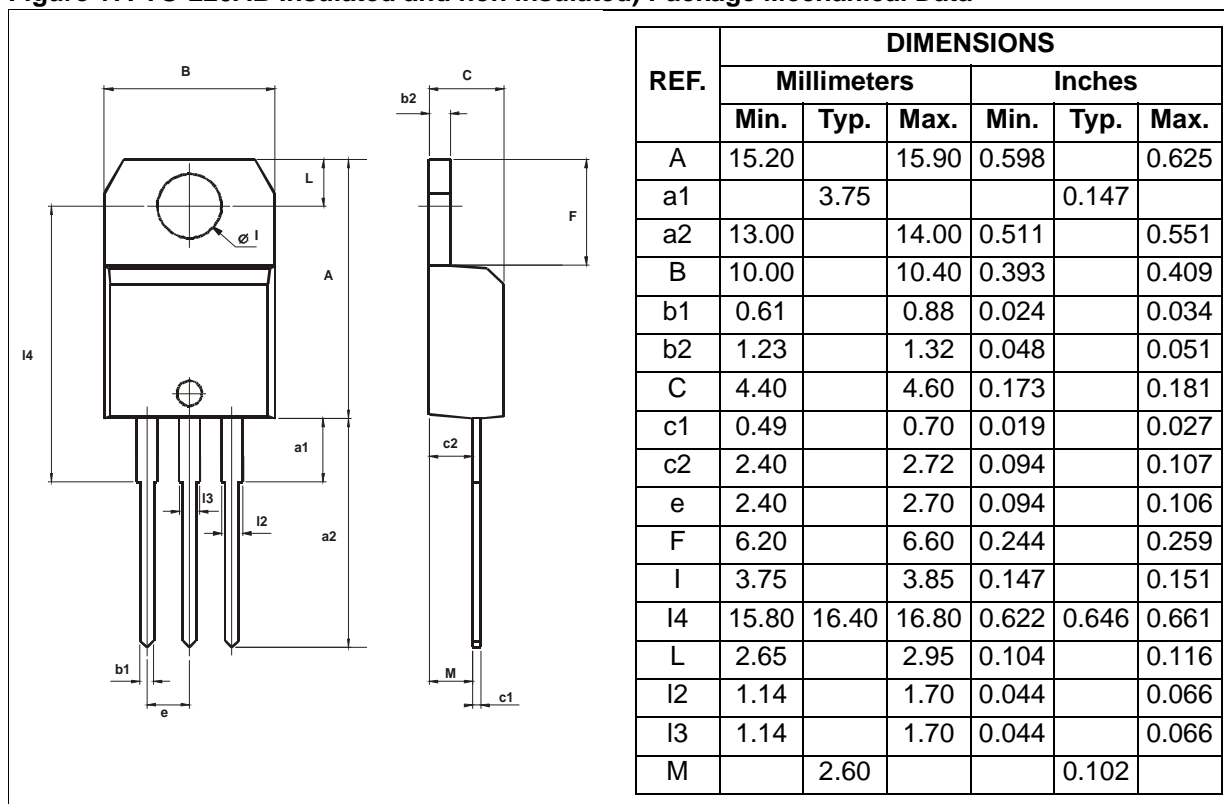


Figure 18: I²PAK Package Mechanical Data

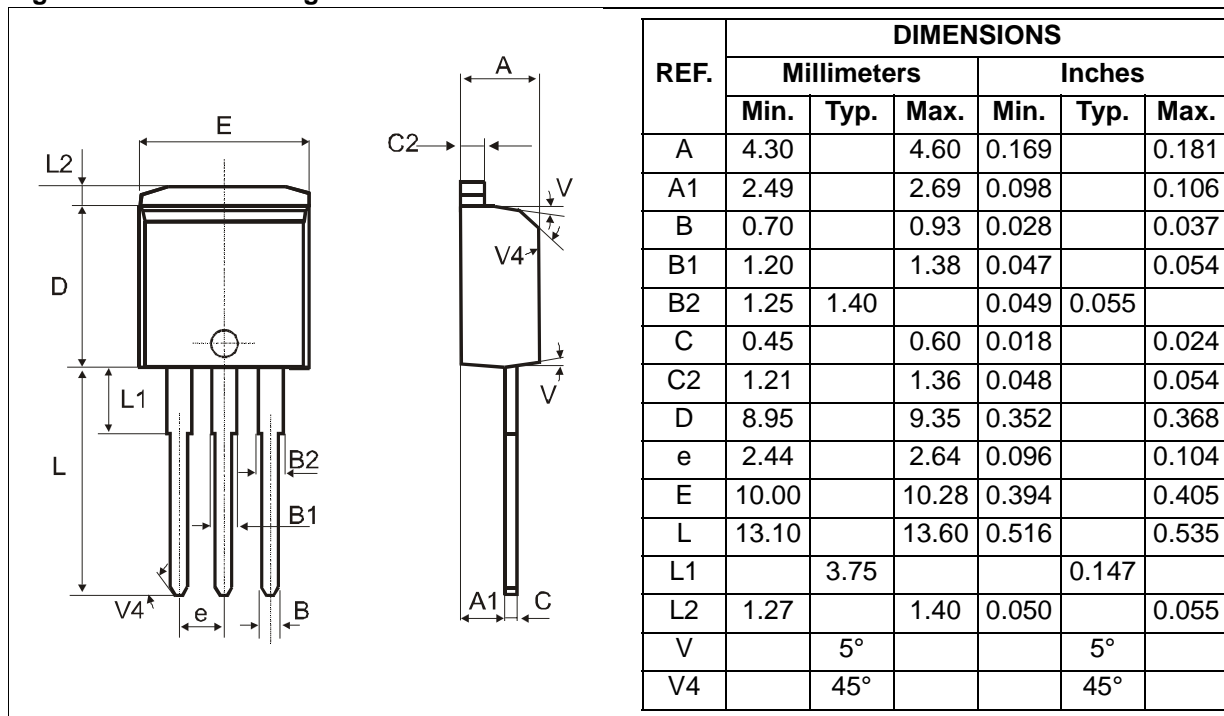


Table 8: Ordering Information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
BTA/BTB12-xxxzyzRG	BTA/BTB12-xxxzyz	TO-220AB	2.3 g	50	Tube
T1205-xxxG	T1205-xxxG	D ² PAK	1.5 g	50	Tube
T1205-xxxG-TR	T1205-xxxG			1000	Tape and reel
T1235-xxxG	T1235xxxG	D ² PAK	1.5 g	50	Tube
T1235-xxxG-TR	T1235xxxG			1000	Tape & reel
T1235-xxxR	T1235-xxxR	I ² PAK	1.5 g	50	Tube

Note: xxx = voltage, yy = sensitivity, z = type

Table 9: Revision History

Date	Revision	Description of Changes
Sep-2002	6A	Last update.
01-Jun-2005	7	1. I ² PAK package added. 2. TO-220AB delivery mode changed from bulk to tube.
28-Jul-2005	8	T1205 added

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America
www.st.com