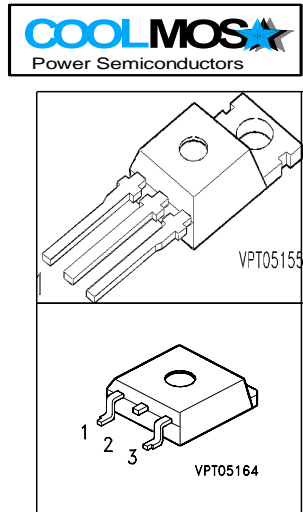
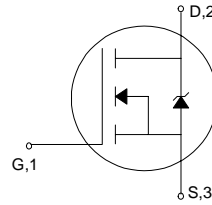


## Cool MOS™ Power-Transistor

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme  $dv/dt$  rated
- Optimized capacitances
- Improved noise immunity
- Former development designation:  
SPPx5N60S5/SPBx5N60S5



Type	$V_{DS}$	$I_D$	$R_{DS(on)}$	Package	Marking	Ordering Code
SPP02N60S5	600 V	1.8 A	3 $\Omega$	P-TO220-3-1	02N60S5	Q67040-S4181
SPB02N60S5				P-TO263-3-2	02N60S5	Q67040-S4212

### Maximum Ratings, at $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current $T_C = 25\text{ }^\circ\text{C}$ $T_C = 100\text{ }^\circ\text{C}$	$I_D$	1.8 1.1	A
Pulsed drain current <sup>1)</sup> $T_C = 25\text{ }^\circ\text{C}$	$I_D \text{ puls}$	3.2	
Avalanche energy, single pulse $I_D = 1.44\text{ A}$ , $V_{DD} = 50\text{ V}$	$E_{AS}$	50	mJ
Avalanche energy (repetitive, limited by $T_{jmax}$ ) $I_D = 1.8\text{ A}$ , $V_{DD} = 50\text{ V}$	$E_{AR}$	0.07	
Avalanche current (repetitive, limited by $T_{jmax}$ )	$I_{AR}$	1.8	A
Reverse diode $dv/dt$ $I_S = 1.8\text{ A}$ , $V_{DS} < V_{DSS}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_{jmax} = 150\text{ }^\circ\text{C}$	$dv/dt$	6	kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$	$\pm 20$	V
Power dissipation $T_C = 25\text{ }^\circ\text{C}$	$P_{tot}$	25	W
Operating and storage temperature	$T_j, T_{stg}$	-55... +150	$^\circ\text{C}$

**Electrical Characteristics**, at  $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

**Thermal Characteristics**

Thermal resistance, junction - case	$R_{thJC}$	-	-	5	K/W
Thermal resistance, junction - ambient (Leaded and through-hole packages)	$R_{thJA}$	-	-	62	
SMD version, device on PCB: @ min. footprint @ 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	62	
		-	35	-	

**Static Characteristics**, at  $T_j = 25\text{ °C}$ , unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0\text{ V}$ , $I_D = 0.25\text{ mA}$	$V_{(BR)DSS}$	600	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D = 80\text{ }\mu\text{A}$ , $T_j = 25\text{ °C}$	$V_{GS(th)}$	3.5	4.5	5.5	
Zero gate voltage drain current, $V_{DS}=V_{DSS}$ $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$ $V_{GS} = 0\text{ V}$ , $T_j = 150\text{ °C}$	$I_{DSS}$	-	0.5	1	$\mu\text{A}$
		-	-	50	
Gate-source leakage current $V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$	$I_{GSS}$	-	-	100	nA
Drain-source on-state resistance $V_{GS} = 10\text{ V}$ , $I_D = 1.1\text{ A}$	$R_{DS(on)}$	-	2.7	3	$\Omega$

<sup>1</sup>current limited by  $T_{jmax}$

<sup>2</sup> Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical without blown air.

**Electrical Characteristics**, at  $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic Characteristics**

Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 1.1A$	-	1.4	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0V$ , $V_{DS} = 25V$ , $f = 1MHz$	-	240	-	pF
Output capacitance	$C_{oss}$		-	77	-	
Reverse transfer capacitance	$C_{rss}$		-	4.4	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 350V$ , $V_{GS} = 10V$ , $I_D = 1.8A$ , $R_G = 50\Omega$	-	35	-	ns
Rise time	$t_r$		-	35	-	
Turn-off delay time	$t_{d(off)}$		-	35	52	
Fall time	$t_f$		-	20	30	

**Gate Charge Characteristics**

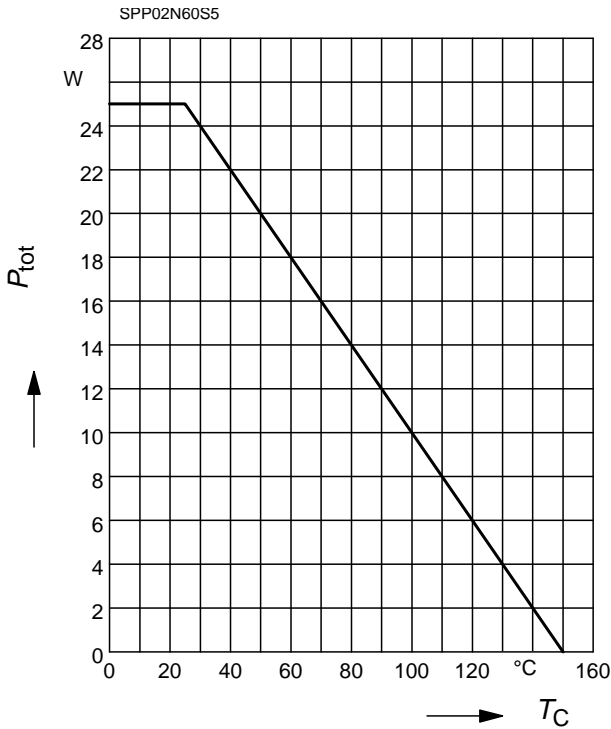
Gate to source charge	$Q_{gs}$	$V_{DD} = 350V$ , $I_D = 1.8A$	-	2.3	-	nC
Gate to drain charge	$Q_{gd}$		-	4.5	-	
Total gate charge	$Q_g$	$V_{DD} = 350V$ , $I_D = 1.8A$ , $V_{GS} = 0$ to $10V$	-	7.3	9.5	

**Reverse Diode**

Inverse diode continuous forward current	$I_S$	$T_C = 25\text{ °C}$	-	-	1.8	A
Inverse diode direct current, pulsed	$I_{SM}$		-	-	3.2	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0V$ , $I_F = 1.8A$	-	1	1.2	V
Reverse recovery time	$t_{rr}$	$V_R = 350V$ , $I_F = I_S$ , $di_F/dt = 100A/\mu s$	-	860	1460	ns
Reverse recovery charge	$Q_{rr}$		-	1.6	-	$\mu C$

**Power dissipation**

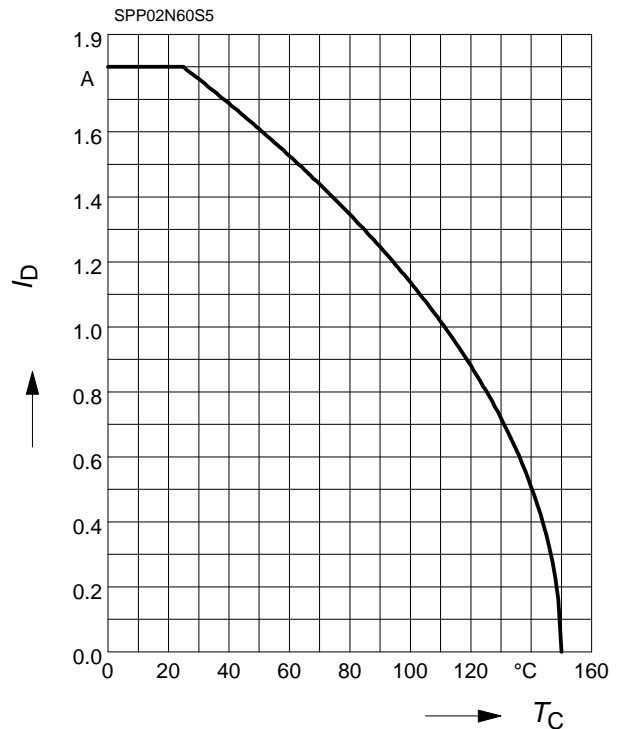
$P_{tot} = f(T_C)$



**Drain current**

$I_D = f(T_C)$

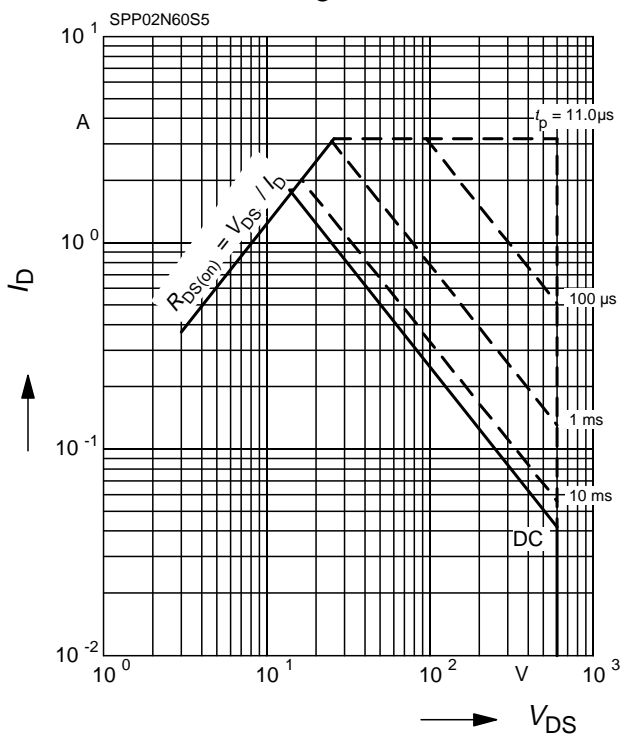
parameter:  $V_{GS} \geq 10\text{ V}$



**Safe operating area**

$I_D = f(V_{DS})$

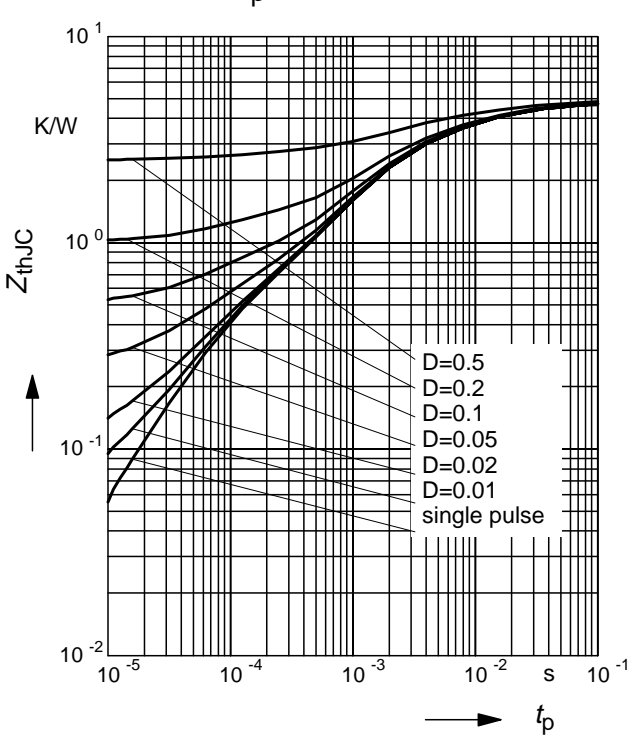
parameter:  $D=0.01, T_C=25^\circ\text{C}$



**Transient thermal impedance**

$Z_{thJC} = f(t_p)$

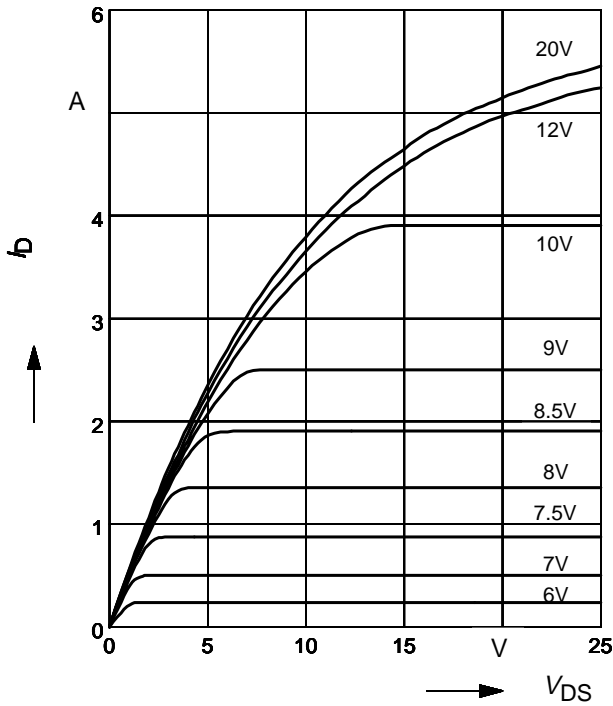
parameter:  $D = t_p / T$



**Typ. output characteristic**

$I_D = f(V_{DS})$

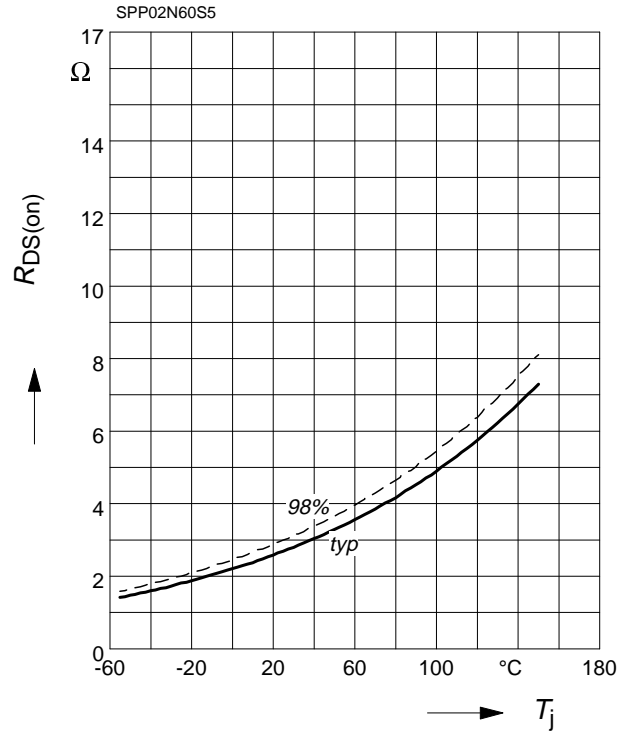
Parameter:  $V_{GS}, T_j = 25\text{ }^\circ\text{C}$



**Drain-source on-resistance**

$R_{DS(on)} = f(T_j)$

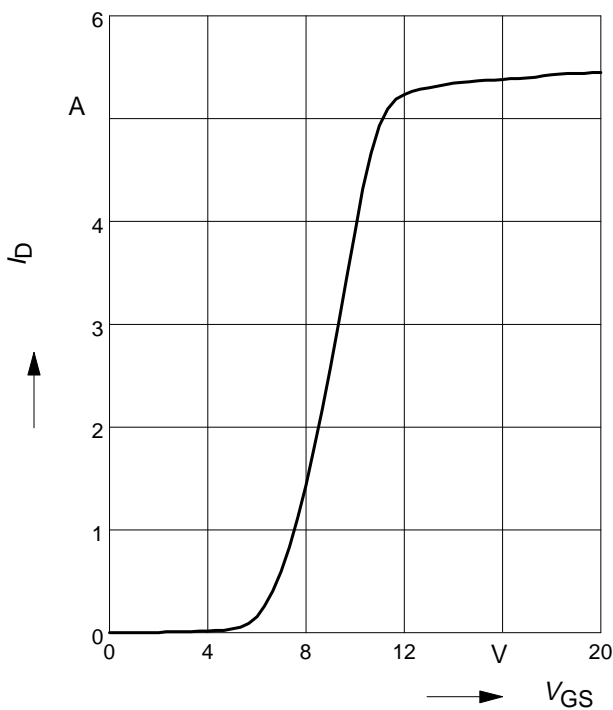
parameter:  $I_D = 1.1\text{ A}, V_{GS} = 10\text{ V}$



**Typ. transfer characteristics**

$I_D = f(V_{GS})$

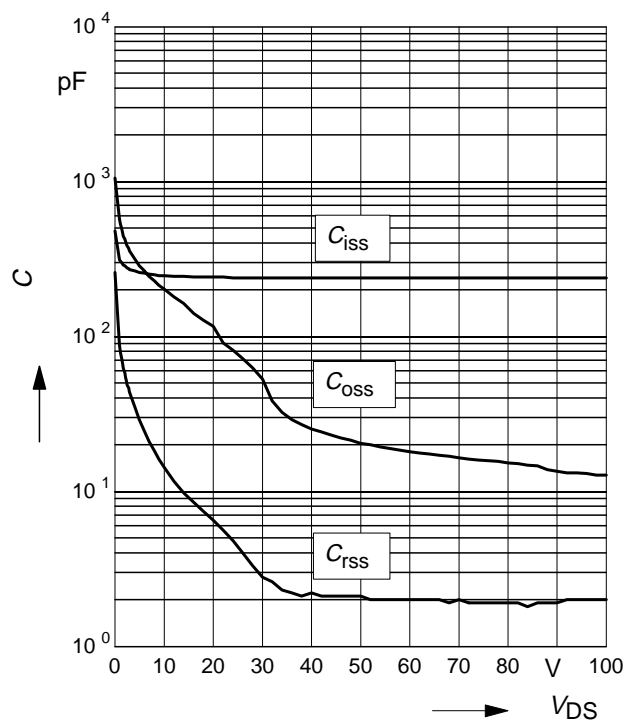
$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$



**Typ. capacitances**

$C = f(V_{DS})$

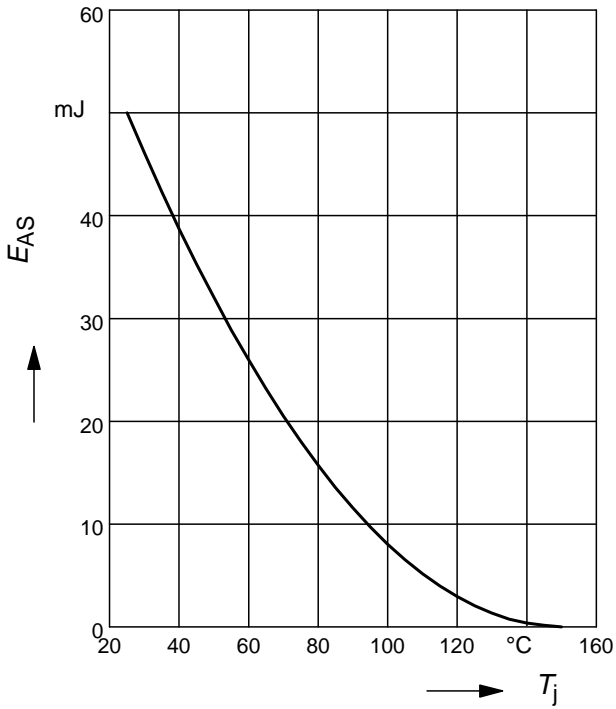
parameter:  $V_{GS} = 0\text{ V}, f = 1\text{ MHz}$



**Avalanche energy**

$$E_{AS} = f(T_j)$$

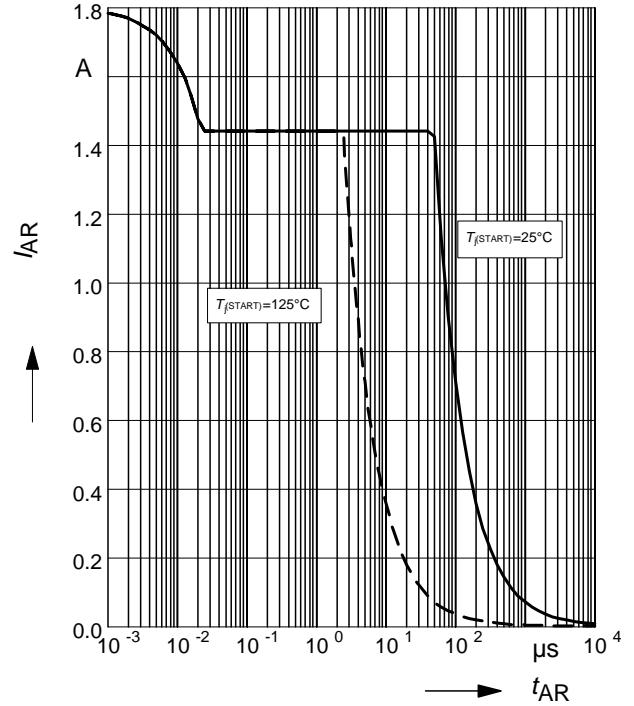
par.:  $I_D=1.44A$ ,  $V_{DD}=50V$



**Avalanche SOA**

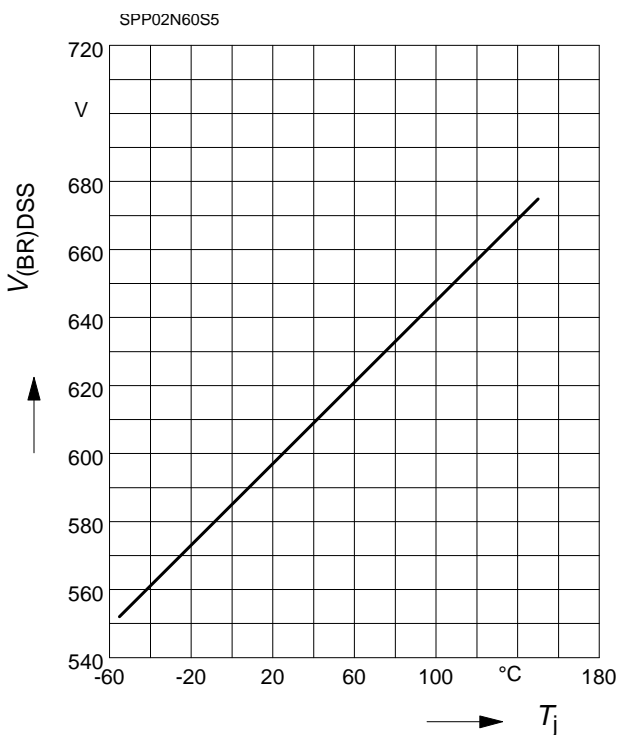
$$I_{AR} = f(t_{AR})$$

par.:  $T_j \leq 150\text{ °C}$



**Drain-source breakdown voltage**

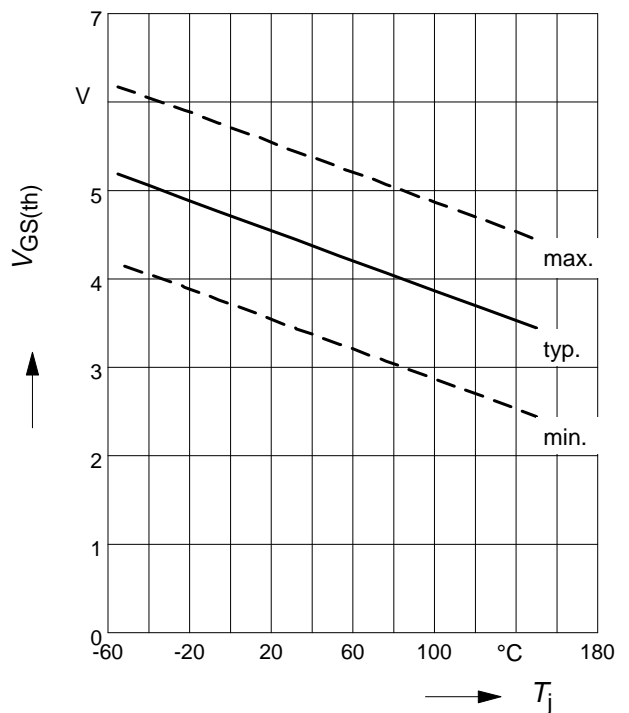
$$V_{(BR)DSS} = f(T_j)$$



**Gate threshold voltage**

$$V_{GS(th)} = f(T_j)$$

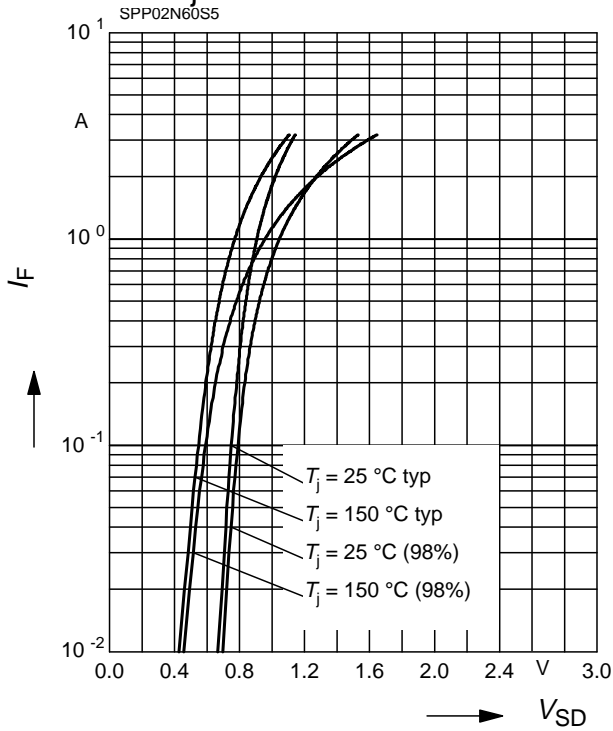
parameter:  $V_{GS} = V_{DS}$ ,  $I_D = 80\text{ μA}$



**Forward characteristics of reverse diode**

$$I_F = f(V_{SD})$$

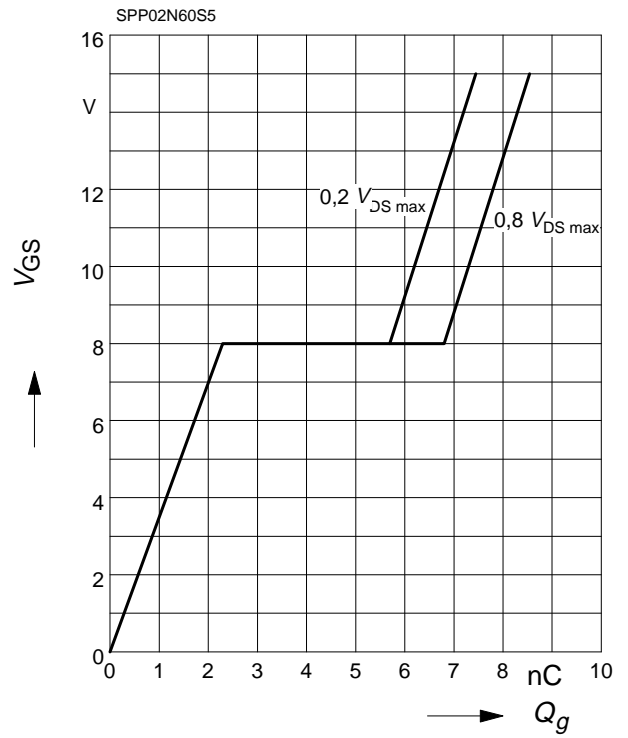
parameter:  $T_j$ ,  $t_p = 10 \mu s$

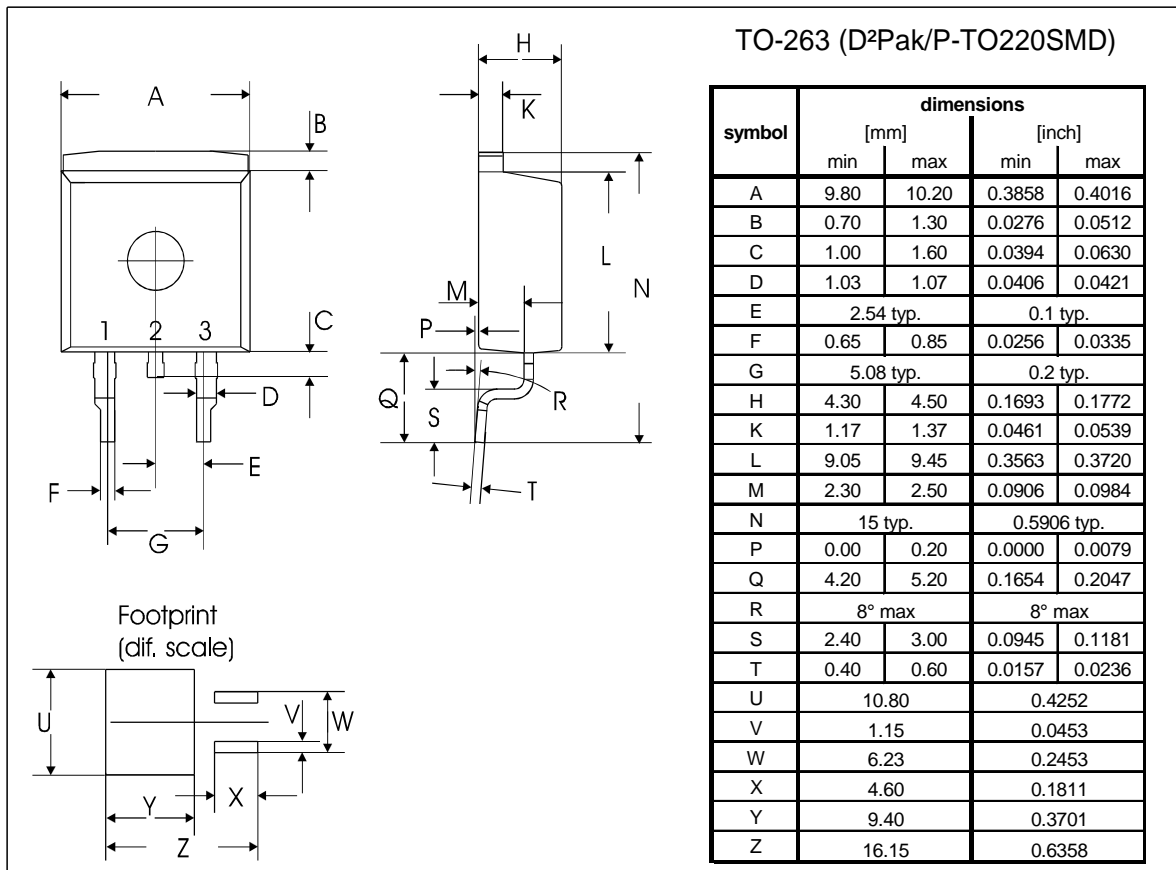
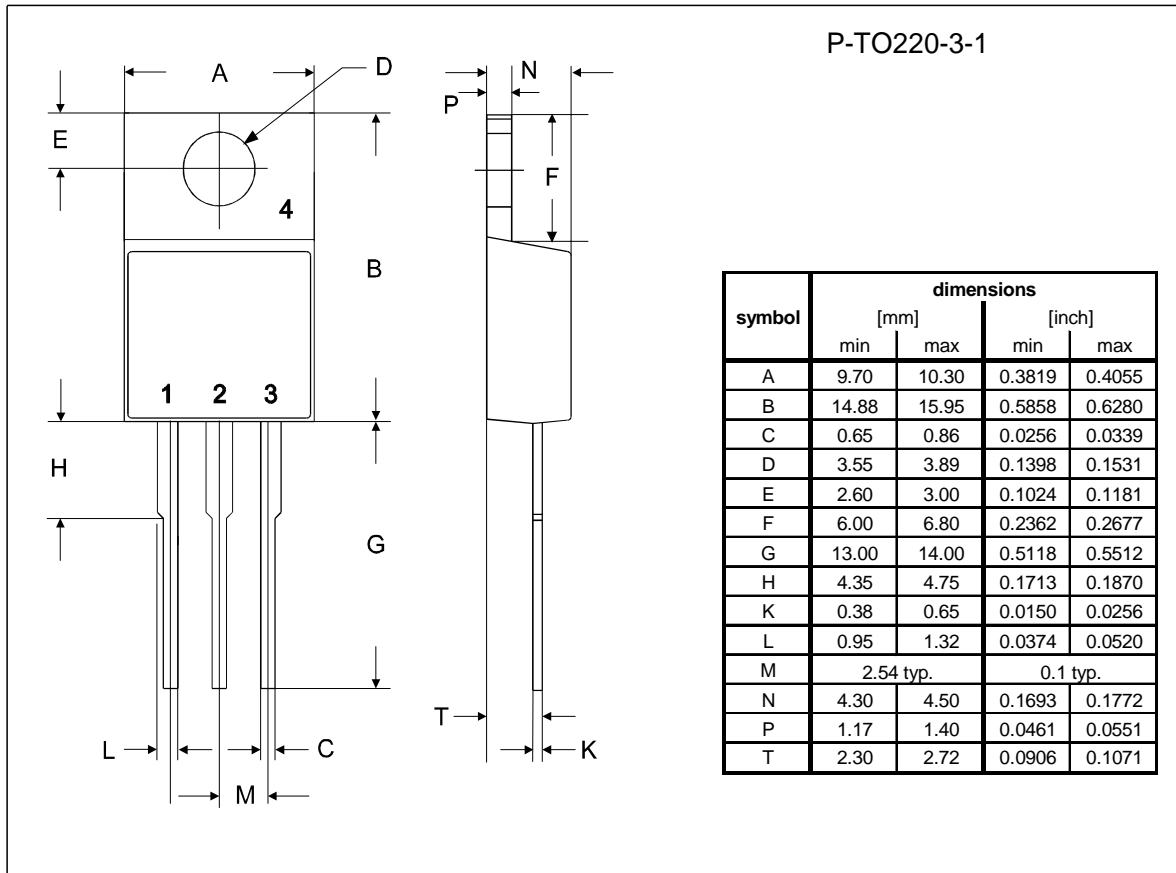


**Typ. gate charge**

$$V_{GS} = f(Q_{Gate})$$

parameter:  $I_D = 1.8 \text{ A pulsed}$







**Published by**  
**Infineon Technologies AG,**  
**Bereichs Kommunikation**  
**St.-Martin-Strasse 53,**  
**D-81541 München**  
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