

CMOS linear image sensor

S10077

Digital output, built-in 8/10-bit AD converter, single power supply operation



S10077 is a CMOS linear image sensor designed for image input applications. The signal processing circuit has a charge amplifier with excellent input/output characteristics. The circuit also includes a 8-bit/10-bit AD converter.

Features

- Pixel pitch: 14 μm
Pixel height: 50 μm
- Number of pixels: 1024 ch
- Single power supply operation: 3.3 to 5 V
- On-chip charge amplifier with excellent input/output characteristics
- Built-in timing generator allows operation with only start and clock pulse inputs
- Video data rate: 1 MHz Max.
- Spectral response range: 400 to 1000 nm
- Digital output
- 8-bit/10-bit switchable ADC
- Simultaneous charge integration and variable integration time function

Applications

- Analytical instrument
- Position detection
- Image reading

■ Absolute maximum ratings

| Parameter | Symbol | Value | Unit |
|---------------------------|---------|------------|------|
| Supply voltage | Vdd | -0.3 to +6 | V |
| AD mode selection voltage | Vsel | -0.3 to +6 | V |
| Clock pulse voltage | V (CLK) | -0.3 to +6 | V |
| Start pulse voltage | V (ST) | -0.3 to +6 | V |
| Operating temperature *1 | Topr | -5 to +60 | °C |
| Storage temperature | Tstg | -10 to +70 | °C |

*1: No condensation

■ Shape specifications

| Parameter | Specification | Unit |
|--------------------|---------------|---------------|
| Number of pixels | 1024 | - |
| Pixel pitch | 14 | μm |
| Pixel height | 50 | μm |
| Active area length | 14.336 | mm |
| Window material | TENPAX | - |

■ Recommended terminal voltage

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------|--------|------------|------|------------|------|
| Supply voltage | Vdd | 3.3 | 5 | 5.25 | V |
| AD mode selection voltage | 10-bit | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | 8-bit | - | 0 | - | V |
| Clock pulse voltage | High | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low | - | 0 | - | V |
| Start pulse voltage | High | Vdd - 0.25 | Vdd | Vdd + 0.25 | V |
| | Low | - | 0 | - | V |

■ Electrical characteristics [Ta=25 °C, Vdd=5 V, V (CLK)=V (ST)=5 V]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|--------|------|------------|------|------|
| Clock pulse frequency | 10-bit | 1 | - | 6 | MHz |
| | 8-bit | 1 | - | 12 | |
| Video data rate | VR | - | f (CLK)/12 | - | kHz |
| Power consumption | P | - | 70 | - | mW |

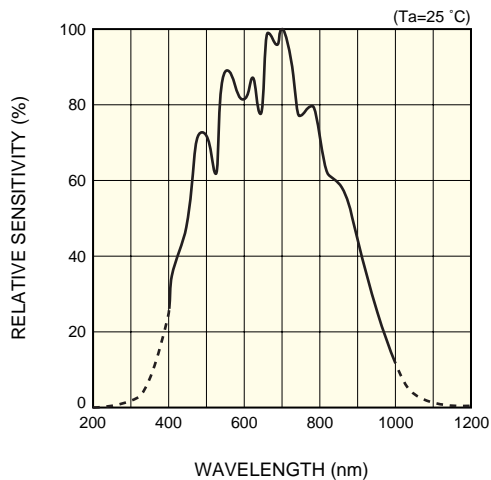
■ Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V (CLK)=V (ST)=5 V]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|-------------|-------------|------|----------|----------------------|
| Spectral response range | λ | 400 to 1000 | | | nm |
| Peak sensitivity wavelength | λ_p | - | 700 | - | nm |
| Photo sensitivity | RES | - | 42 | - | V/ μJcm^2 |
| Dark current | ID | - | 0.7 | - | fA |
| Saturation output voltage *2 | Vsat | - | 3.3 | - | V |
| Readout noise | Nr | - | 0.7 | - | digit |
| Offset output voltage | Vo | - | 0.3 | - | V |
| Photo response non-uniformity *3 *4 | PRNU | - | - | ± 10 | % |

*2: Relative voltage when Vo is taken as reference value

*3: Uniformity is defined under the condition that the device is uniformly illuminated by light which is 50 % of the saturation exposure level and using 1022 pixels excluding both ends pixels as follows:

■ Spectral response (typical example)



■ AD converter specifications (Ta=25 °C)

| Parameter | Symbol | Specification | Unit |
|-----------------------------|-------------|---------------|------|
| Digital output format | - | Serial output | - |
| Resolution *5 | 10-bit mode | 10 | bit |
| | 8-bit mode | 8 | |
| Conversion voltage range *6 | - | 0 to 3.3 | V |

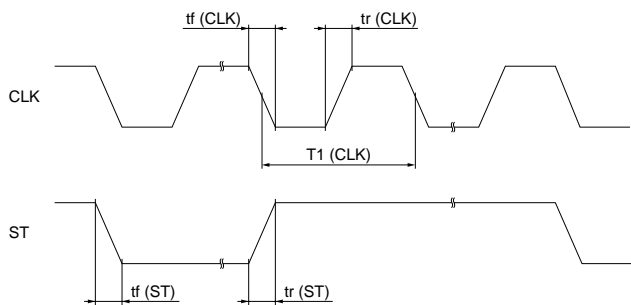
*5: Vsel=5 V (10-bit mode), 0 V (8-bit mode)

*6: Digital output is available from MSB as serial output.

10-bit mode: D9 to D0

8-bit mode: D7 to D0

■ Timing chart



KMPDC0224EA

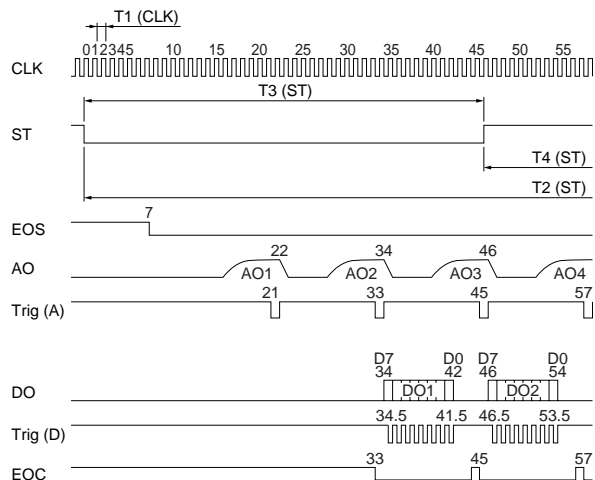
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------|--------------------|-------|------|------|------|
| Clock pulse rise and fall time | tr (CLK), tf (CLK) | 0 | 20 | 30 | ns |
| Start pulse time cycle | T2 (ST) | 12339 | - | - | CLK |
| Start pulse low time | T3 (ST) | 45 | - | - | CLK |
| Start pulse high time *7 | T4 (ST) | 3600 | - | - | CLK |
| Start pulse rise and fall time | tr (ST), tf (ST) | 0 | 20 | 30 | ns |

*7: Signal charge integration time equals the High period of start pulse + 7 CLK cycles.

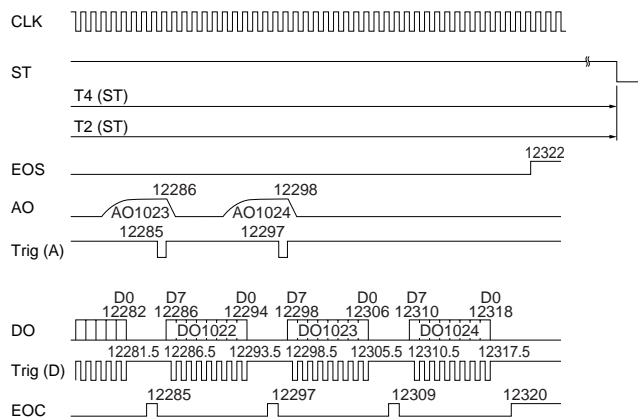
The shift register operation starts at the rise of CLK pulse immediately after ST pulse sets to low.
Integration time can be changed by changing the High-to-Low ratio of ST pulses.

8-bit mode

● In the neighborhood of start pixel



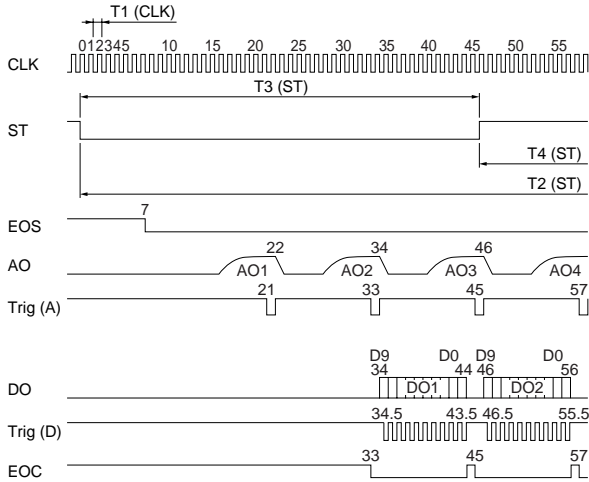
● In the neighborhood of last pixel



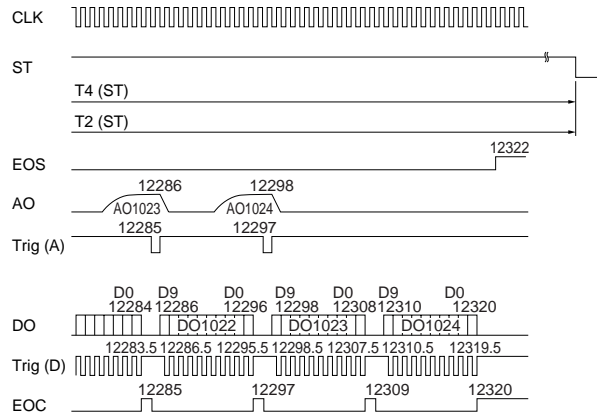
KMPDC0225EA

10-bit mode

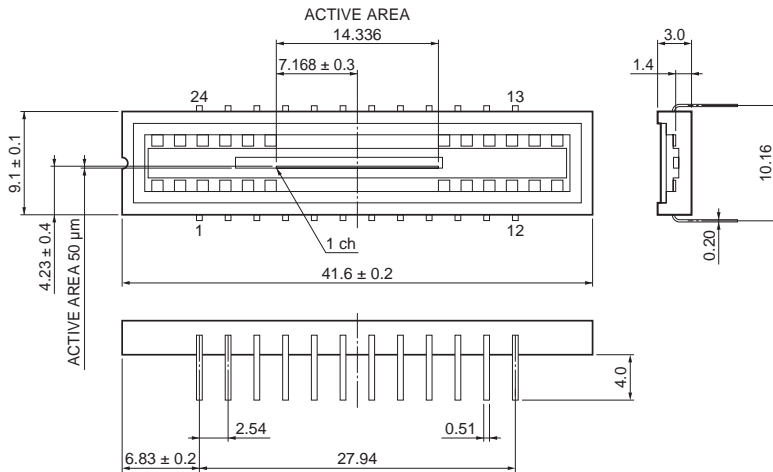
● In the neighborhood of start pixel



● In the neighborhood of last pixel

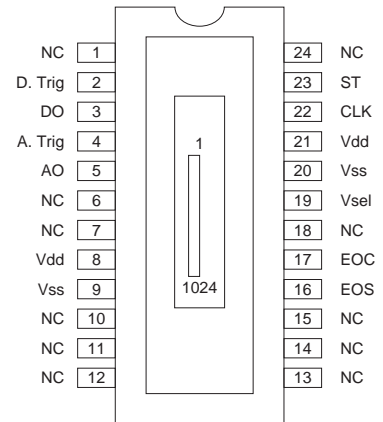


■ Dimensional outline (unit: mm, tolerance unless otherwise noted: ±0.1)



Package: LCP (Liquid Crystalline Polymer)

■ Pin connection



KMPDC0228EA

KMPDA0202EA

KMPDC0231EA

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---------|---------|-----------------------------------|---------|--------|-------------------------------|
| 1 | NC | No connection | 13 | NC | No connection |
| 2 | D. Trig | Trigger signal for digital output | 14 | NC | No connection |
| 3 | DO | Digital output | 15 | NC | No connection |
| 4 | A. Trig | Trigger signal for analog output | 16 | EOS | End of scan signal |
| 5 | AO | Analog output | 17 | EOC | Digital conversion end signal |
| 6 | NC | No connection | 18 | NC | No connection |
| 7 | NC | No connection | 19 | Vsel | AD mode selection voltage |
| 8 | Vdd | Supply voltage | 20 | Vss | GND |
| 9 | Vss | GND | 21 | Vdd | Supply voltage |
| 10 | NC | No connection | 22 | CLK | Clock signal |
| 11 | NC | No connection | 23 | ST | Start signal |
| 12 | NC | No connection | 24 | NC | No connection |

HAMAMATSU

Information furnished by HAMAMATSU is believed to be reliable. However, no responsibility is assumed for possible inaccuracies or omissions. Specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein. ©2005 Hamamatsu Photonics K.K.

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Hamamatsu City, 435-8558 Japan, Telephone: (81) 053-434-3311, Fax: (81) 053-434-5184, www.hamamatsu.com

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658

France: Hamamatsu Photonics France S.A.R.L.: 8, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Smidsvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741

Cat. No. KMPD1088E01
Jul. 2005 DN