283-617

W24257

Winbond Electronics Corp.

32K × 8 CMOS STATIC RAM

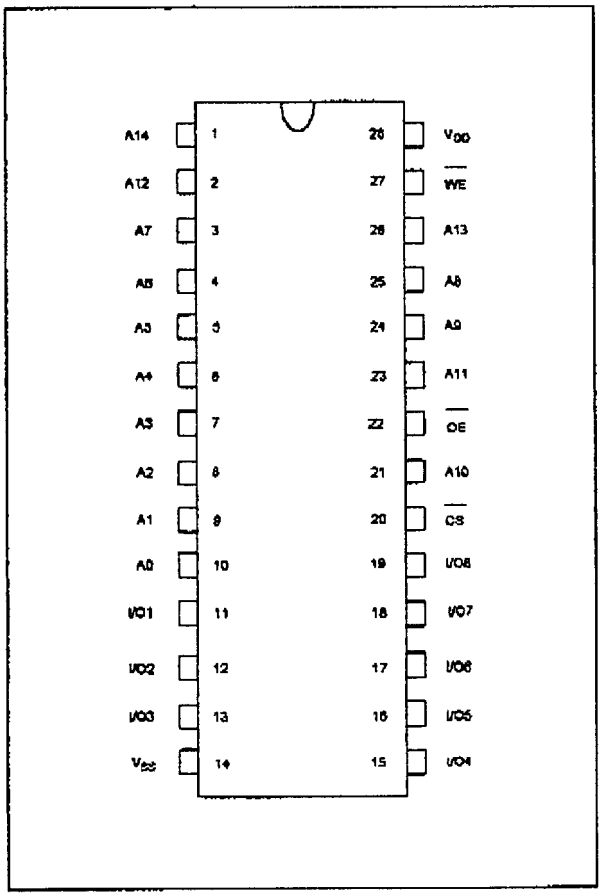
8GENERAL DESCRIPTION

The W24257 is a slow speed, low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

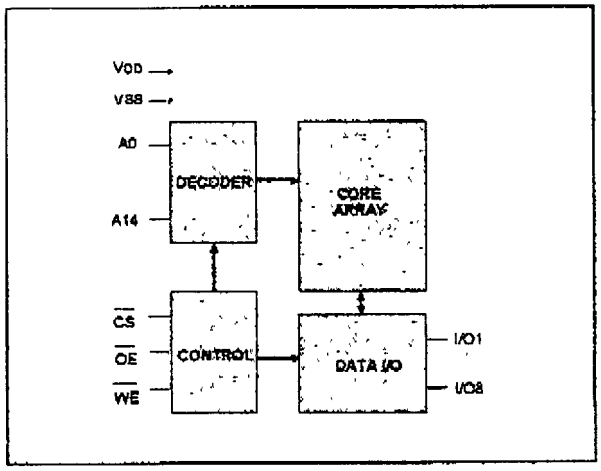
FEATURES

- Low power consumption:
  - Active: 400 mW (max.)
  - Standby: 250 µW (max.) (LL-version)
    500 µW (max.) (L-version)
- Access time: 70/100 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min)
- Available packages: 28-pin 600 mil DIP, 330 mil SOP, 300 mil skinny DIP and SOJ

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

Publication Release Date: April 1997
Revision A11

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TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1–I/O8	V_{DD} CURRENT
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to +7.0	V
Input/Output to Vss Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

Operating Characteristics

(V_{DD} = 5V ±10%, Vss = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{DD}		-2	-	+2	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = Vss to V_{DD}, $\overline{CS}$ = V_{IH} (min.) or $\overline{OE}$ = V_{IH} (min.) or $\overline{WE}$ = V_{IL} (max.)		-2	-	+ 2	µA
Output Low Voltage	V_{OL}	I_{OL} = +4.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL} (min.), I/O = 0 mA	70	-	-	60	mA
		Cycle = min., Duty = 100%	100	-	-	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} (min.) Cycle = min., Duty = 100%		-	-	3	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{DD} -0.2V	LL	-	-	50	µA
			L	-	-	100	µA

Note: Typical characteristics are at V_{DD} = 5V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

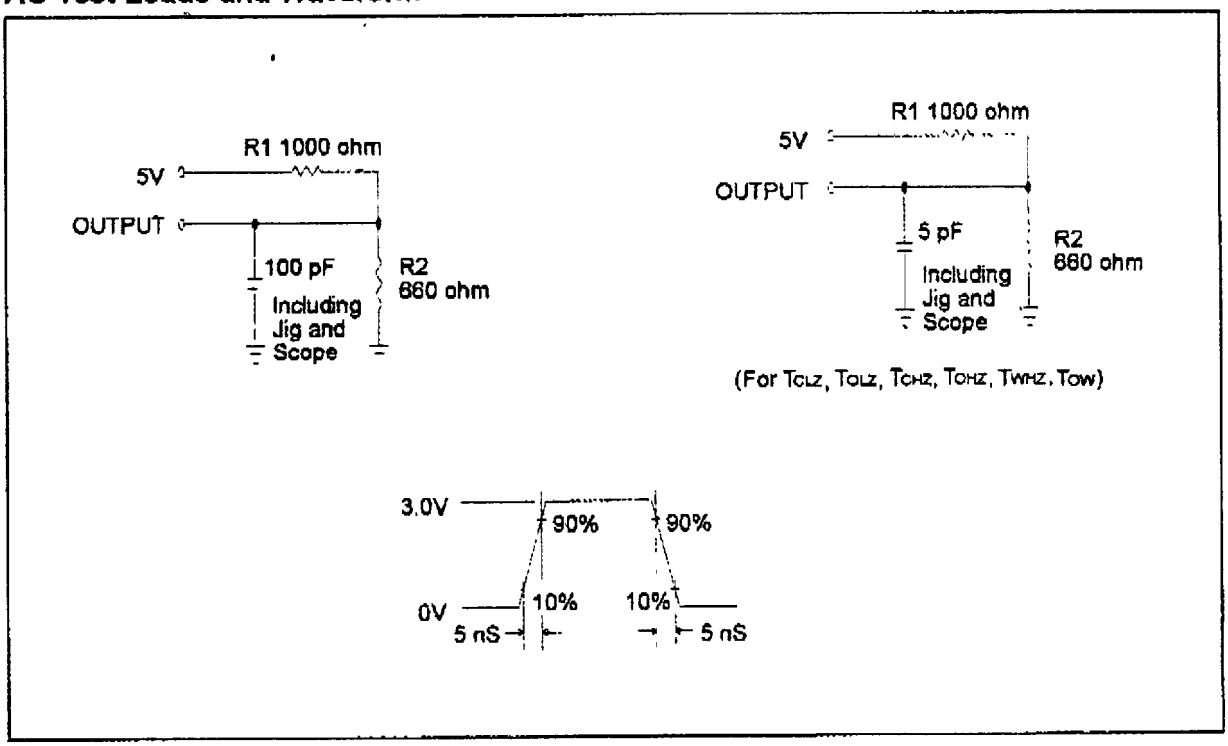
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.8V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 100 pF, I_{OH}/I_{OL} = -1 mA/4 mA

AC Test Loads and Waveform



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AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYM.	W24257-70		W24257-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	100	-	nS
Address Access Time	T_{AA}	-	70	-	100	nS
Chip Select Access Time	T_{ACS}	-	70	-	100	nS
Output Enable to Output Valid	T_{AOE}	-	35	-	50	nS
Chip Selection to Output in Low Z	T_{CLZ}*	10	-	10	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	30	-	35	nS
Output Disable to Output in High Z	T_{OHZ}*	-	30	-	35	nS
Output Hold from Address Change	T_{OH}	10	-	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

PARAMETER		SYM.	W24257-70		W24257-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	100	-	nS
Chip Selection to End of Write		T_{CW}	60	-	80	-	nS
Address Valid to End of Write		T_{AW}	60	-	80	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	45	-	60	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	T_{WR}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	30	-	40	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	30	-	30	nS
Output Disable to Output in High Z		T_{OHZ}*	-	30	-	30	nS
Output Active from End of Write		T_{OW}	0	-	0	-	nS

* These parameters are sampled but not 100% tested

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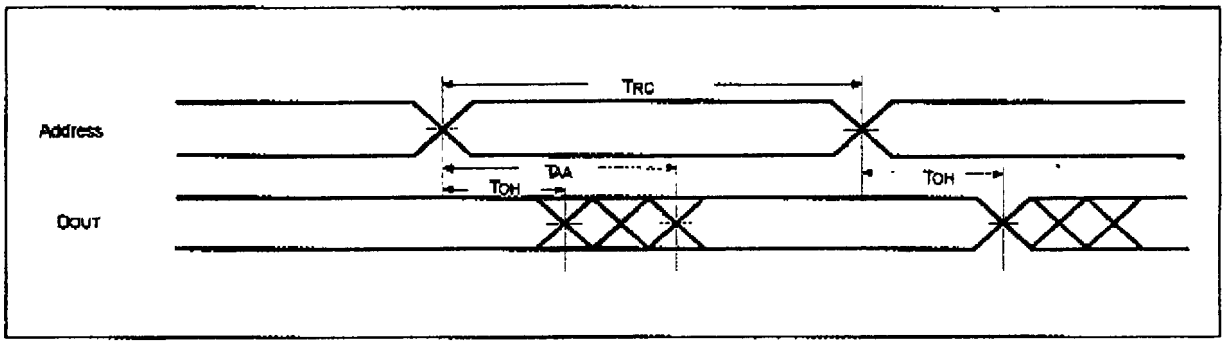
TIMING WAVEFORMS

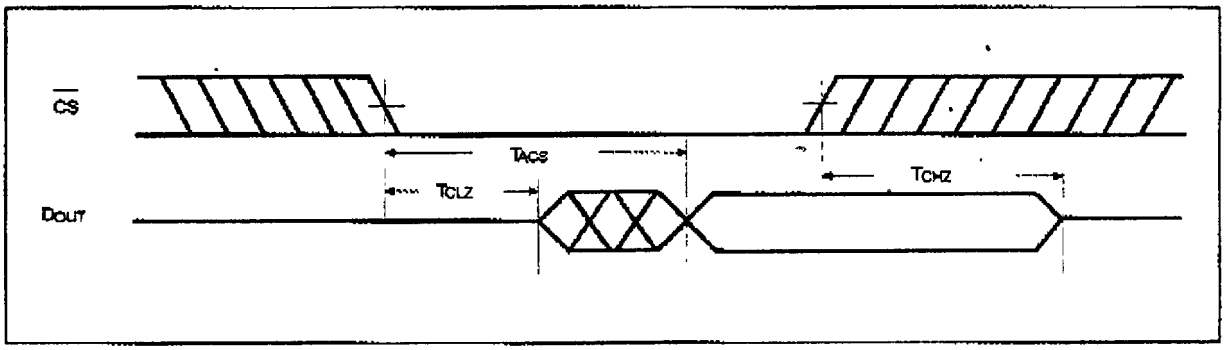
Read Cycle 1

(Address Controlled)



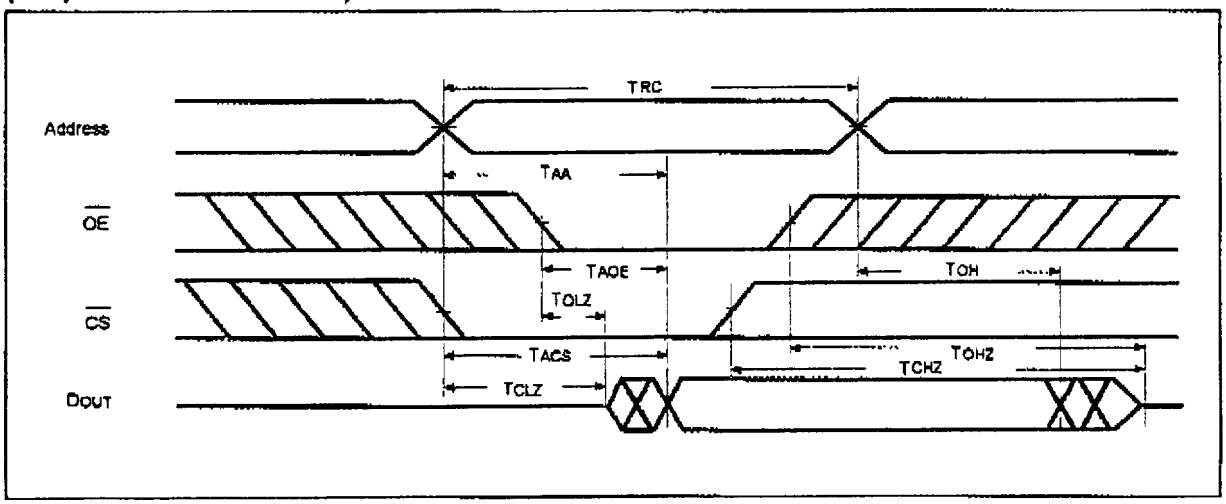
Read Cycle 2

(Chip Select Controlled)



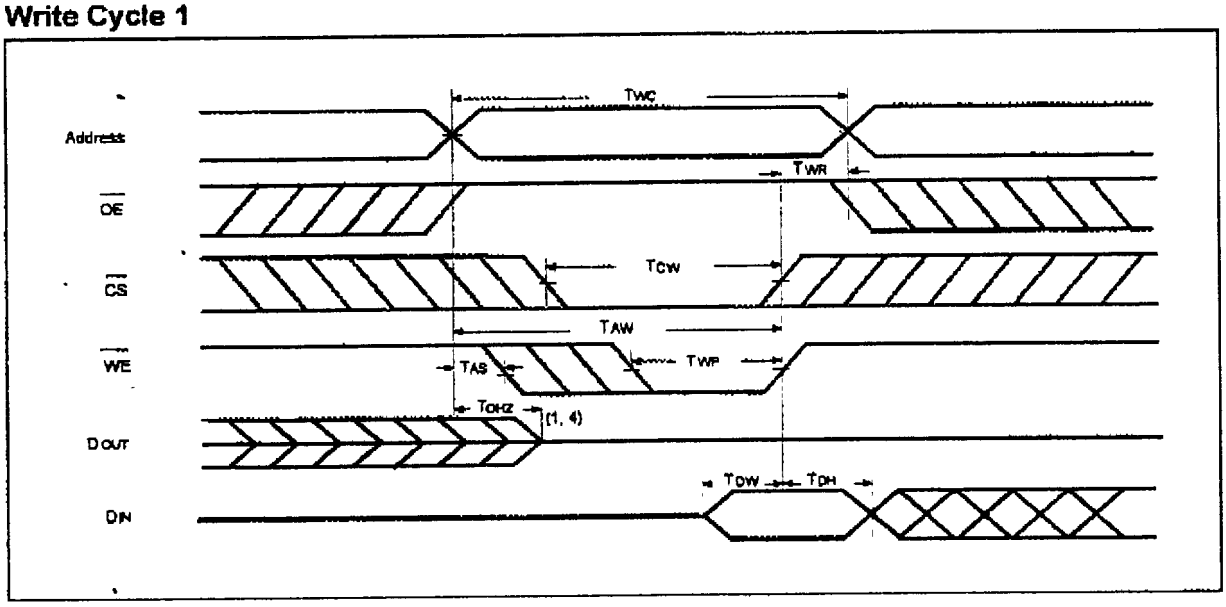
Read Cycle 3

(Output Enable Controlled)



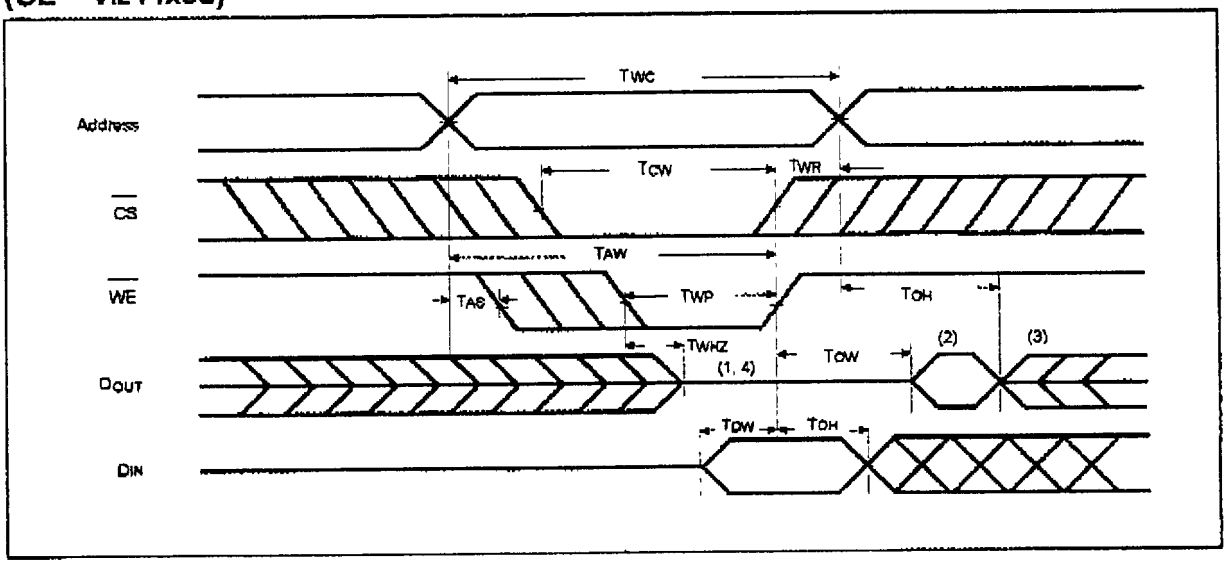
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

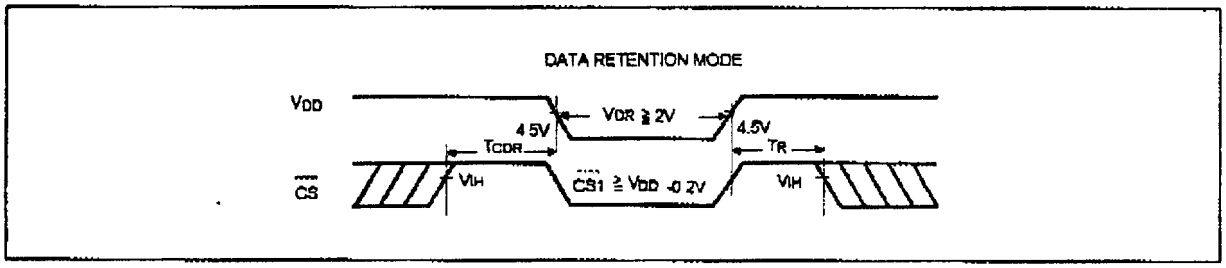
DATA RETENTION CHARACTERISTICS

(T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS} \geq V_{DD}$ -0.2V		2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS} \geq V_{DD}$ -0.2V	LL	-	-	20	µA
		V_{DD} = 3V	L	-	-	50	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention		0	-	-	nS
Operation Recovery Time	T_R	waveform		T_{RC}*	-	-	nS

T_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24257-70LL	70	80	50	600 mil DIP
W24257-70L	70	80	100	600 mil DIP
W24257-10L	100	70	100	600 mil DIP
W24257S-70LL	70	80	50	330 mil SOP
W24257S-70L	70	80	100	330 mil SOP
W24257S-10L	100	70	100	330 mil SOP
W24257K-70LL	70	80	50	300 mil Skinny
W24257K-70L	70	80	100	300 mil Skinny
W24257K-10L	100	70	100	300 mil Skinny
W24257J-70LL	70	80	50	300 mil SOJ
W24257J-70L	70	80	100	300 mil SOJ
W24257J-10L	100	70	100	300 mil SOJ

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

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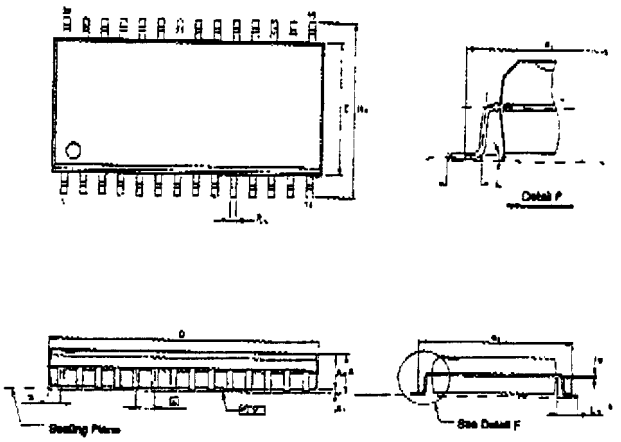
Package Dimensions, continued

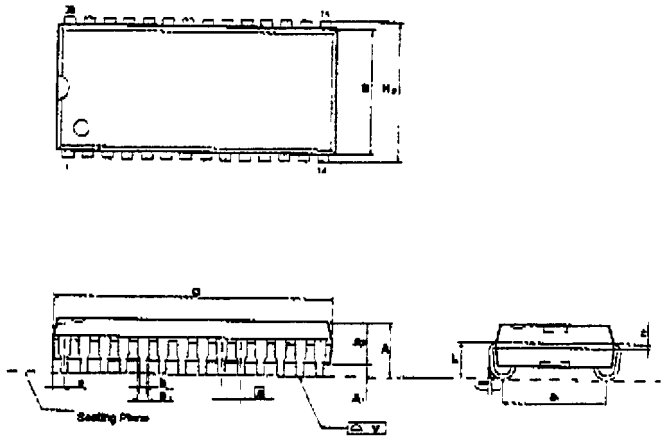
28-pin SO Wide Body



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A_1	0.004	—	—	0.10	—	—
A_2	0.088	0.098	0.103	2.36	2.49	2.62
b	0.014	0.018	0.020	0.36	0.41	0.51
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.728	—	18.11	18.52
E	0.326	0.331	0.335	8.20	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H_D	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.038	0.044	0.71	0.91	1.12
L_C	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0	—	10

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and determined at the mold parting line
4. Controlling dimension: Inches
5. General appearance spec. should be based on final visual inspection spec.

28-pin Small Outline J Band



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.027	—	—	0.69	—	—
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.009	0.010	0.014	0.20	0.25	0.36
D	—	0.710	0.730	—	18.03	18.54
E	0.295	0.300	0.305	7.49	7.62	7.75
e	0.044	0.050	0.056	1.12	1.27	1.42
θ_1	0.245	0.265	0.285	6.22	6.73	7.24
H_D	0.327	0.337	0.347	8.31	8.56	8.81
L	0.077	0.087	0.097	1.96	2.21	2.46
S	—	—	0.045	—	—	1.14
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line
4. Controlling dimension: Inches.
5. General appearance spec. should be based on final visual inspection spec.

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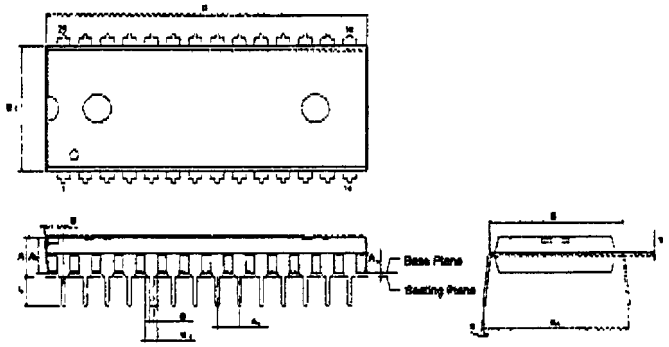
PACKAGE DIMENSIONS

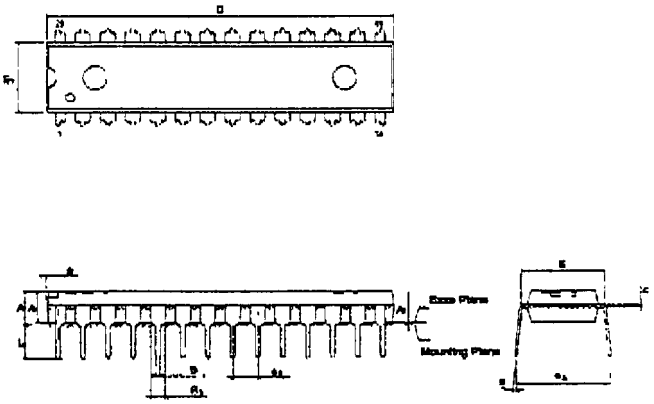
28-pin P-DIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	11.72	13.84	13.97
e	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: inches.
6. General appearance spec. should be based on final visual inspection spec.

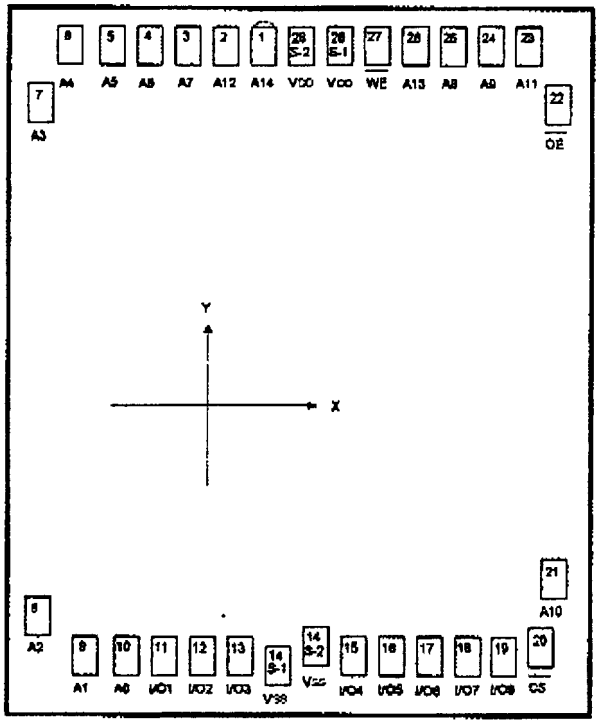
28-pin P-DIP Skinny



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.380	1.400	—	35.05	35.56
E	0.300	0.310	0.320	7.62	7.87	8.13
E_1	0.283	0.288	0.293	7.19	7.32	7.44
e	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0°	—	15°	0°	—	15°
e_A	0.330	0.350	0.370	8.38	8.89	9.40
S	—	—	0.055	—	—	1.40

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: inches.
6. General appearance spec. should be based on final visual inspection spec.

BONDING PAD DIAGRAM



PAD NO.	X	Y
1	-127.08	2785.05
2	-377.73	2785.05
3	-628.38	2785.05
4	-879.03	2785.05
5	-1129.68	2785.05
6	-1380.33	2785.05
7	-1686.51	2640.06
8	-1682.01	-2645.91
9	-1448.10	-2802.51
10	-1090.80	-2802.51
11	-877.32	-2807 28
12	-627.84	-2807.28
13	-349.56	-2807.28
14S-1	-155.52	-2781.00
14S-2	-7.02	-2771.64
15	249.21	-2807.28
16	498.69	-2807.28
17	776.97	-2807.28
18	1026.45	-2807.28
19	1304.73	-2807.28
20	1689.30	-2802.51
21	1686.51	-2520.90
22	1686.51	2644.74
23	1459.17	2785.05
24	1208.52	2785.05
25	957.87	2785.05
26	707.22	2785.05
27	456.57	2785.05
28S-1	205.92	2771.55
28S-2	21.42	2780.91

Note: For bare chip form (C.O B) applications, the substrate must be connected to VDD or left floating in the PCB layout.