TEXAS INSTRUMENTS

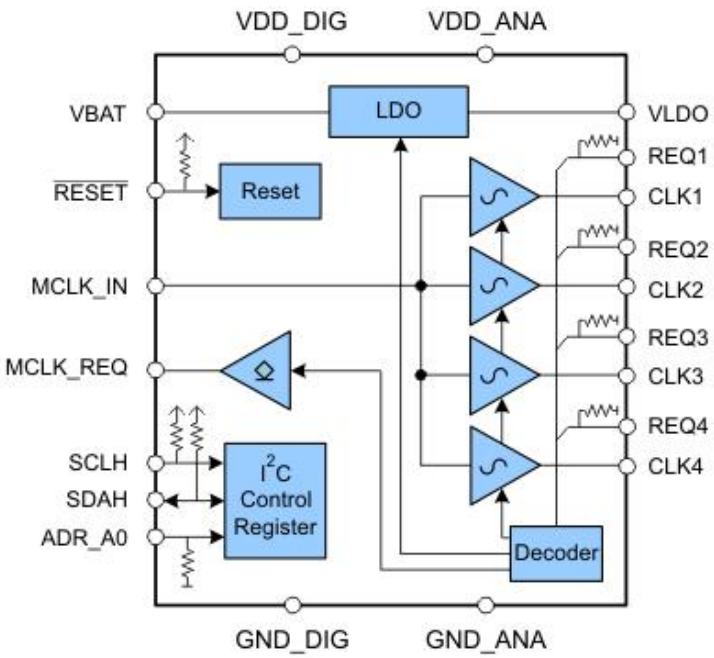
CDC3S04 Quad Sine-Wave Clock Buffer

General Description:

The CDC3S04 is a four-channel low-power low-jitter sine-wave clock buffer. It can be used to buffer a single master clock to multiple peripherals. The four sine-wave outputs (CLK1–CLK4) are designed for minimal channel-to-channel skew and ultralow additive output jitter.

Each output has its own clock request inputs which enables the dedicated clock output. These clock requests are active-high (can also be changed to be active-low via I2C), and an output signal is generated that can be sent back to the master clock to request the clock (MCLK_REQ). MCKL_REQ is an open-source output and supports the wired-OR function (default mode). It needs an external pulldown resistor. MCKL_REQ can be changed to wired-AND or push-pull functionality via I2C.

Key Features:



- 1:4 Low-Jitter Clock Buffer
- Single-Ended Sine-Wave Clock Input and Outputs
- Ultralow Phase Noise and Standby Current
- Individual Clock Request Inputs for Each Output
- On-Chip Low-Dropout Output (LDO) for Low-Noise TCXO Supply
- Serial I2C Interface (Compatible With High-Speed Mode, 3.4 Mbit/s)
- 1.8-V Device Power Supply
- Wide Temperature Range, –30°C to 85°C
- ESD Protection: 2 KV HBM, 750 V CDM, and 100 V MM
- Small 20-Pin Chip-Scale Package: 0.4-mm Pitch WCSP (1.6 mm × 2 mm)

Applications:

- Cellular Phones
- Smart Phones

- Mobile Handsets
- Portable Systems
- Wireless Modems Including GPS, WLAN, W-BT, D-TV, DVB-H, FM Radio, WiMAX, and System Clock

Related Products Information:

Mfr Part #	Farnell #	Newark #	Description
CDC3S04YFFR	1783261	51R1160	CDC3S04 Quad Sine-Wave Clock Buffer