ULTRA-PRECISION 1:4 LVPECL FANOUT BUFFER/TRANSLATOR WITH INTERNAL TERMINATION

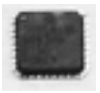
Precision Edge® SY89831U

FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - **DC-to > 2.0GHz throughput**
  - **<450ps propagation delay (IN-to-Q)**
  - **< 20ps within-device skew**
  - **< 225ps rise/fall time**
- **Ultra-low jitter design:**
  - **< 1ps$_{RMS}$ cycle-to-cycle jitter**
  - **< 1ps$_{RMS}$ random jitter**
  - **< 10ps$_{PP}$ deterministic jitter**
  - **< 10ps$_{PP}$ total jitter (clock)**
- **Unique patent-pending input termination and VT pin accepts DC- and AC-coupled differential inputs**
- **800mV, 100K LVPECL output swing**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **Industrial temperature range: –40°C to +85°C**
- **Available in 16-pin (3mm ×3mm) MLF™ package**

APPLICATIONS

- **Processor clock distribution**
- **SONET clock distribution**
- **Fibre Channel clock distribution**
- **Gigabit Ethernet clock distribution**



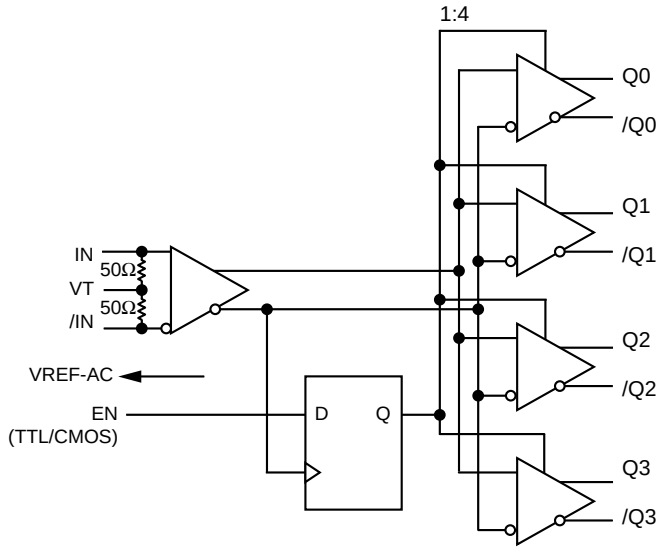
Precision Edge®

DESCRIPTION

The SY89831U is a high-speed, 2GHz differential LVPECL 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps (5ps typ.) over supply voltage and temperature. The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF–AC reference output is included for AC-coupled applications.

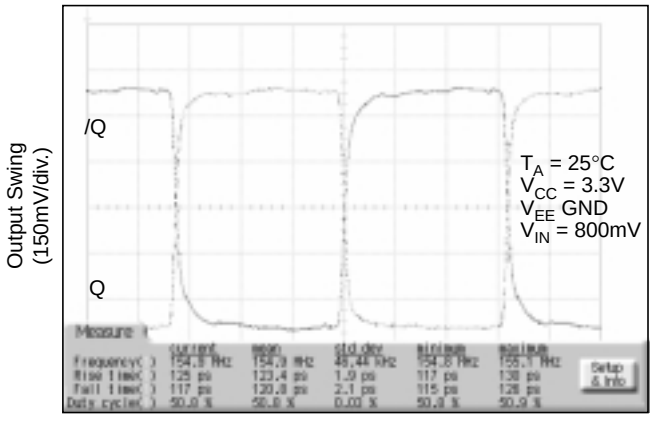
The SY89831U is a part of Micrel's high-speed clock synchronization family. For applications that require a different I/O combination, consult Micrel's website at www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE

155MHz Output



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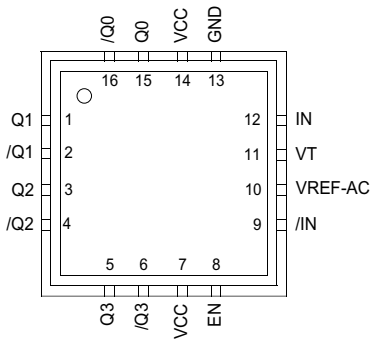
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



16-Pin MLF™ (MLF-16)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89831UMI	MLF-16	Industrial	831U	Sn-Pb
SY89831UMITR[2]	MLF-16	Industrial	831U	Sn-Pb
SY89831UMG[3]	MLF-16	Industrial	831U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89831UMGTR[2, 3]	MLF-16	Industrial	831U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
15, 16 1, 2, 3, 4, 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	Differential 100K LVPECL Outputs: These LVPECL outputs are the precision, low skew copies of the inputs. Please refer to the "Truth Table" section for details. Unused output pairs may be left open. Terminate wtih 50Ω to V_{CC}–2V. See "Output Termination Recommendations" section for more details.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signs as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an intermediate state if left open. Pleae refer to the "Input Interface Applications" section for more details.
10	VREF–AC	Reference Voltage: These outputs bias to V_{CC}–1.4V. They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.01µF low ESR capacitor to V_{CC}. See "Input Interface Applications" section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more detaiils.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each VCC pin as possible.

TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0[1]	1[1]

Note:

1. On next negative transition of the input signal (IN).

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.5V
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or Sink Current on (IN, /IN) ..... ±50mA
VREF-AC Current
  Source or Sink Current on (I_{VT}) ..... ±2mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage Range ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  MLF™
  (θ_{JA}) Still-Air ..... 60°C/W
  (Ψ_{JB}) Junction-to-Board ..... 32°C/W

DC ELECTRICAL CHARACTERISTICS[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375 3.0		2.625 3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		47	70	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	**Note 5**	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	see Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN – /IN|	see Figure 1b.	0.2			V
$V_{REF–AC}$	Output Reference Voltage		V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

LVTTL/LVCMOS INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.375V to 3.60V; V_{EE} = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		20	µA
I_{IL}	Input LOW Current		–300			µA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in stil-air number, unless otherrwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS[6]

V_{CC} = +2.5V ±5% or +3.3V ±10%; R_L = 50Ω to V_{CC} –2V; T_A = –40°C to +85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage (Q, /Q)		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage (Q, /Q)		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	1100	1600		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[6]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Voltage		–125		30	µA
I_{IL}	Input LOW Voltage		–300			µA

Notes:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[7]

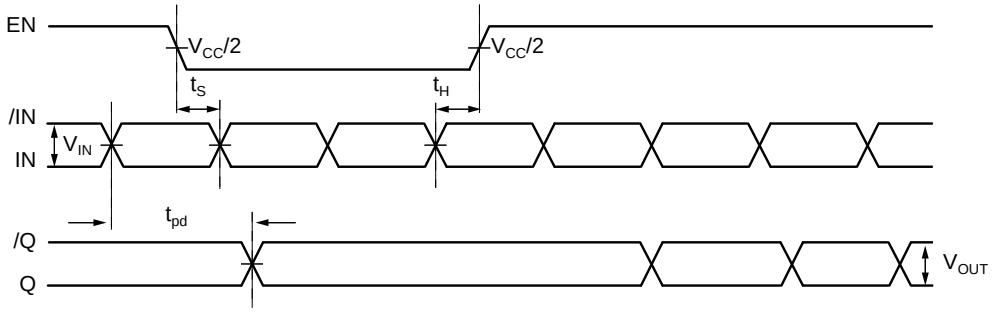
V_{CC} = +2.5V ±5% or +3.3V ±10%; R_L = 50Ω to V_{CC} –2V; T_A = –40°C to +85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	$V_{OUT} \geq 450mV$	2.0	2.5		GHz
t_{pd}	Propagation Delay IN-to-Q	$V_{IN} \geq 100mV$		390		ps
	IN-to-Q	$V_{IN} \geq$ 800mV	250	350	450	ps
t_{SKEW}	Within-Device Skew	**Note 8**		5	20	ps
	Part-to-Part Skew	**Note 9**			150	ps
t_S	Set-Up Time EN to IN, /IN	**Note 10**	300			ps
t_H	Hold Time EN to IN, /IN	**Note 10**	300			ps
t_{JITTER}	Data Random Jitter (RJ) Deterministic Jitter (DJ)	 **Note 11** **Note 12**			 1 10	 ps_{RMS} ps_{PP}
	Clock Cycle-to-Cycle Jitter Total Jitter (TJ)	 **Note 13** **Note 14**			 1 10	 ps_{RMS} ps_{PP}
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	70	150	225	ps

Notes:

7. High-frequency AC parameters are guaranteed by design and characterization.
8. Within device skew is measured between two different outputs under identical input transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
10. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.
11. Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.
12. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
13. Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input frequency of $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

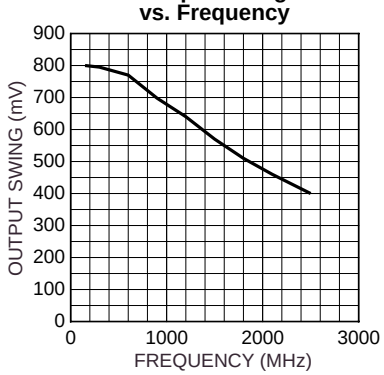
TIMING DIAGRAM



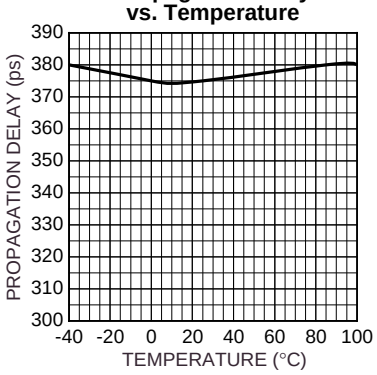
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, R_L = 50Ω to V_{CC}–2V, T_A = 25°C, unless otherwise stated.

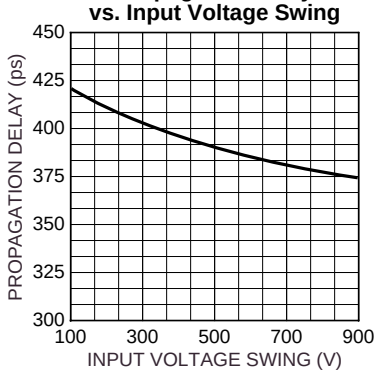
Output Swing vs. Frequency



Propagation Delay vs. Temperature



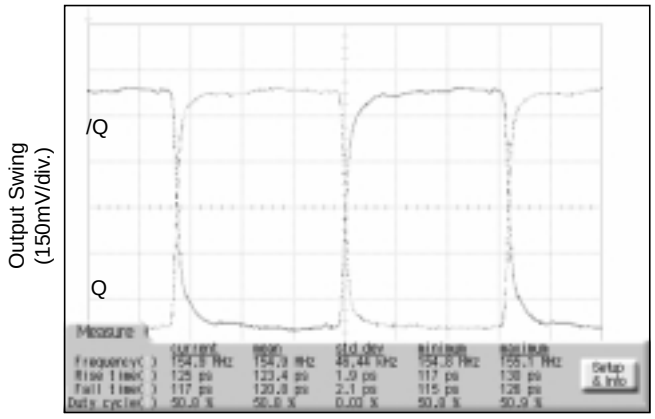
Propagation Delay vs. Input Voltage Swing



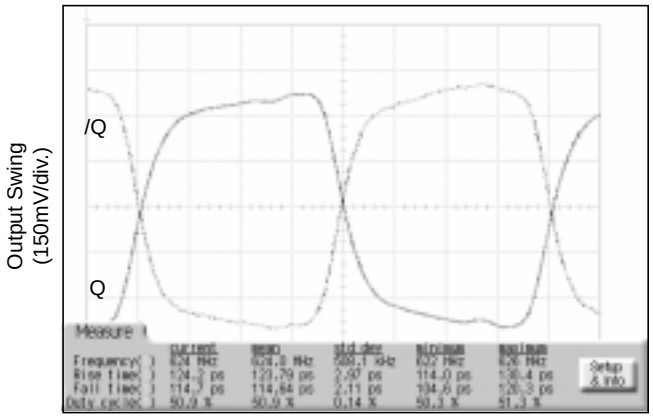
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, V_{IN} = 800mV, R_L = 50Ω to V_{CC}–2V, T_A = 25°C, unless otherwise stated.

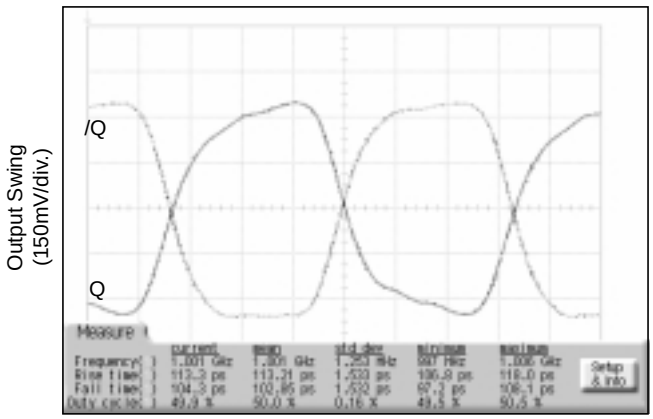
155MHz Output



622MHz Output



1GHz Output



SINGLE-ENDED AND DIFFERENTIAL SWINGS

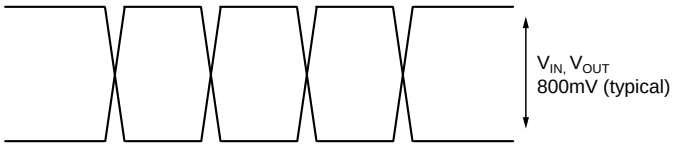


Figure 1a. Single-Ended Swing

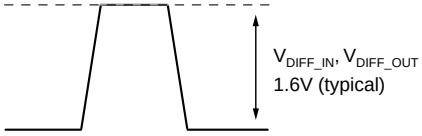


Figure 1b. Differential Swing

INPUT AND OUTPUT STAGES

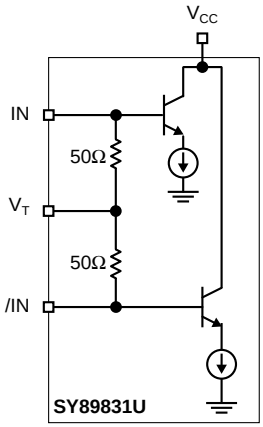


Figure 2a. Simplified Differential

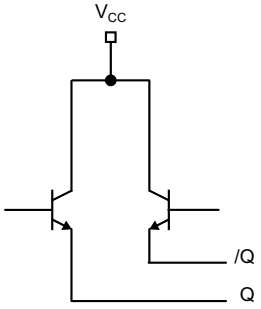


Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS

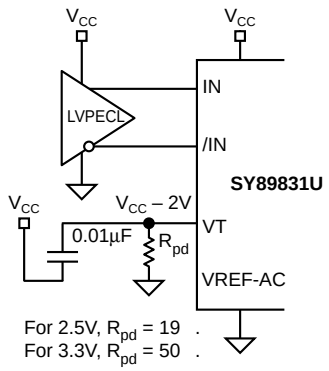


Figure 3a. DC-Coupled LVPECL Input Interface

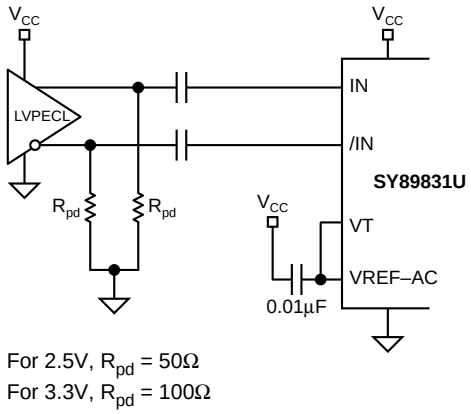


Figure 3b. AC-Coupled LVPECL Input Interface

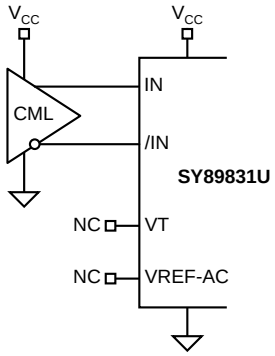


Figure 3c. DC-Coupled CML Input Interface

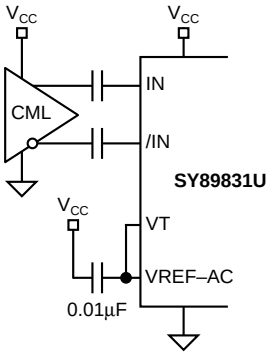


Figure 3d. AC-Coupled CML Input Interface

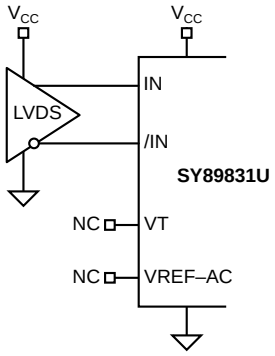


Figure 3e. LVDS Interface

OUTPUT TERMINATION RECOMMENDATIONS

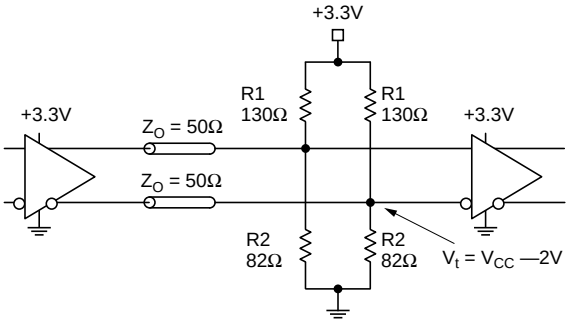


**Figure 4. Parallel Termination—
Thevenin Equivalent**

Note:

1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

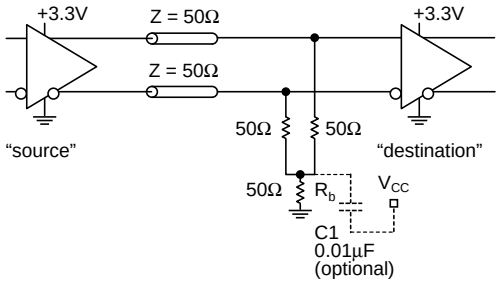


Figure 5. Three-Resistor "Y-Termination"

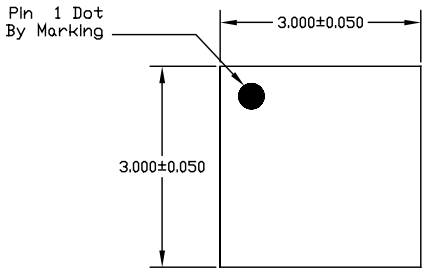
Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_t.
   For +2.5V systems R_b = 19Ω.
4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

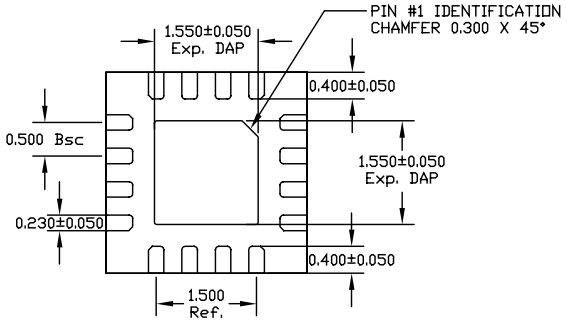
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89830U	1:4 LVPECL Fanout Buffer w/2:1 MUX Input	www.micrel.com/product-info/products/sy89830u.shtml
SY89832U	2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination	www.micrel.com/product-info/products/sy89832u.shtml
SY89833U	3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination	www.micrel.com/product-info/products/sy89833u.shtml
SY89834U	2.5/3.3V Two Input, 1GHz LVTTL/CMOS-to-LVPECL 1:4 Fanout Buffer/Translator	www.micrel.com/product-info/products/sy89833u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0301.pdf

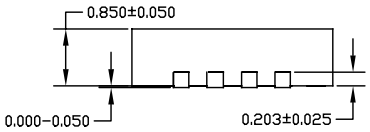
16 LEAD EPAD *Micro*LeadFrame™ (MLF-16)



TOP VIEW

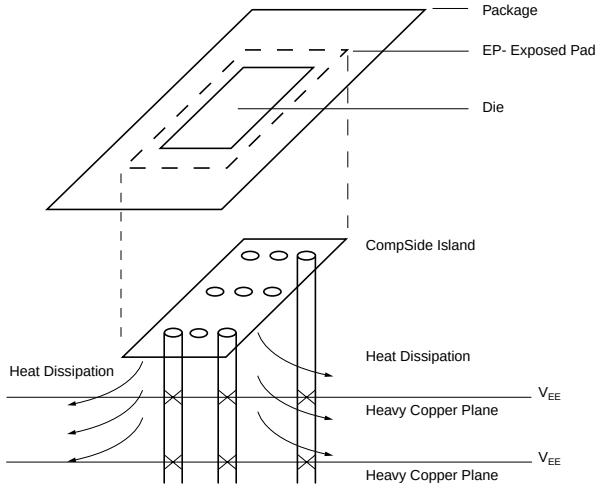


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
Note 2. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

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