

# nanoNET TRX Complementary Dispersive Delay Line (CDDL) DS1804C

Datasheet

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Chirp it.



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**CAUTION!** Electrostatic Sensitive Device. Precaution should be used when handling the device in order to prevent permanent damage.



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# 1 Definition of the CDDL

The Complementary Dispersive Delay Line (CDDL) uses a highly sophisticated SAW (Surface Acoustic Wave) filter device that incorporates two filters within a single device. It is required for the operation of the nanoNET TRX Transceiver.

While most devices have two ports, the CDDL consists of three ports, as shown below.

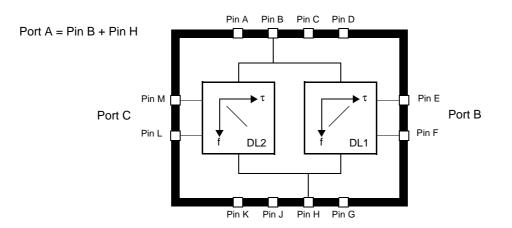


Figure 1: Complementary Dispersive Delay Line schematic

#### Upchirp and Downchirp

Port A is the common input port. The group delay of the filter from the input to one of the outputs is characteristic for these filters.

The respective impulse response for the dispersive Delay Line 2 (DL2) is an *Upchirp* (Linear frequency modulation, where frequency increases in time).

The other output is complementary to this, meaning that the impulse response for Delay Line 1 (DL1) is a *Downchirp* (Linear frequency modulation, where frequency decreases in time).

Within the *nanoNET* system, the CDDL is responsible for distinguishing between two possible incoming signals generated by another *nanoNET TRX Transceiver*. This received signal is either an Upchirp or a Downchirp. Both of these signals have the same center frequency and the same bandwidth so that the difference occurs only in the phase information.

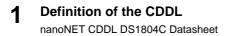
This phase information is enough for the CDDL to compress a pulse at one output port and expand it at the other (that is, to extend the incoming signal to the doubled duration). In this way the CDDL acts like a matched filter for one of the possible transmitted pulses.

#### Balanced Mode

Also, within the *nanoNET* system, the CDDL is directly connected to an RF transceiver. As this transceiver has a differential output and input, the filter is used in a **balanced mode**.

According to this balanced mode, the housing has 6 signal pins – two on each side and two in the center on opposite sides. The detailed pinning is described on the *Balanced Filter (Bottom View)* on page 3 and *Pad Landing (Top View) – Proposal* on page 4. All other pins are connected to ground and at least one of them should be connected with the ground of the PC board.

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Pin Number	Description			
A	GND			
В	A <sub>p</sub> , (port A, line P)			
С	GND			
D	GND			
E	B <sub>n</sub> , (port B, line N)			
F	B <sub>p</sub> , (port B, line P)			
G	GND			
Н	A <sub>n</sub> , (port A, line N)			
J	GND			
к	GND			
L	C <sub>p</sub> , (port C, line P)			
М	C <sub>n</sub> , (port C, line N)			



# 2 CDDL Detailed Description

### 2.1 Balanced Filter (Top View)

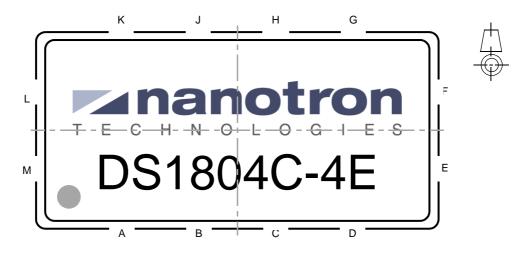


Figure 2: CDDL balanced filter - top view

# 2.2 Balanced Filter (Bottom View)

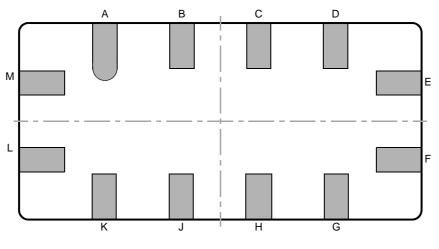


Figure 3: CDDL balanced filter - bottom view

The types of signals for each pin of the CDDL housing is described in the following table.

Table 2: Pin signal types

Туре	Label		
Signal	B, E, F, H, L, M		
Ground	A, C, D, G, I, K, S/R <sup>1</sup>		

1. S/R means seal ring



# 2.3 Housing Layout Dimensions

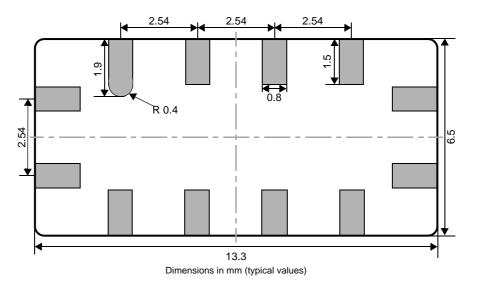
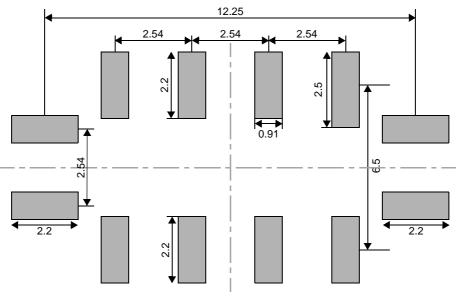


Figure 4: CDDL - bottom view measures

# 2.4 Pad Landing (Top View) – Proposal



Dimensions in mm (typical values)

Figure 5: CDDL pad landing

# 2.5 CDDL on PC board (Top View)

In the illustration below, the signal pins are connected to strip lines. They are designed with a width of 0.91 mm to be able to go through two pins to connect both lines of port A from one side. On a typical PC board (FR4 of height 0.51 mm and copper thickness 35 mm,  $\mathcal{E}_r = 4.7$ ) the impedance of these lines is about 50  $\Omega$ .

Note: The ground pins, which are connected with ground, are not shown in the following figure.

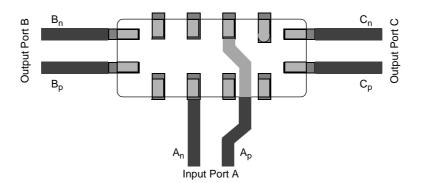
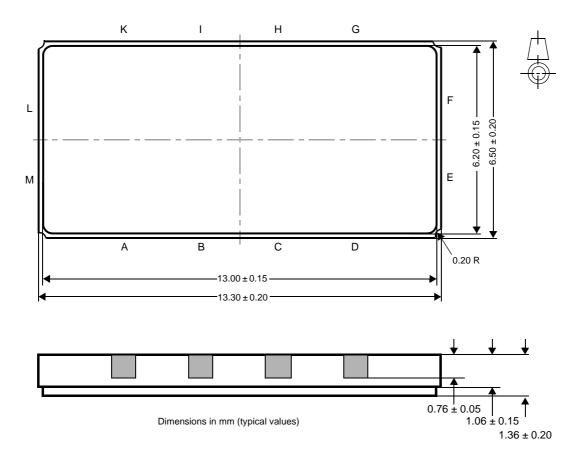
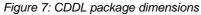


Figure 6: CDDL test board connections

### 2.6 Package Dimensions







# **3** Measurements

### 3.1 Test Board for Measurements

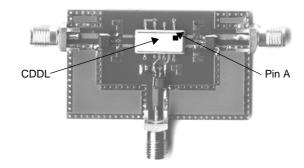


Figure 8: Test board used by Nanotron with 3 baluns (ETC1-1-13, Impedance ratio 1:1)

# 3.2 Target Specifications and Measurement Results (03/2003)

Parameter	Symbol	Conditions	Min	Typical	Max	Measured	Unit	
Center Frequency <sup>1</sup>	f <sub>0</sub>	-	247	250	253	249.51	MHz	
Average insertion <sup>2</sup> loss without matching	_	VSWR <sub>in</sub> SWR <sub>out</sub>	_	33	35	32.7	dB	
3 dB bandwidth <sup>3</sup>	В	-	85	88	91	88.7	MHz	
Average gradient of dispersion <sup>4</sup>	K <sub>d</sub>	-	12.0	12.5	13.0	12.81	μs/ GHz	
Nominal group delay	τ <sub>delay</sub>	= K <sub>d</sub> B	1.02	1.1	1.18	1.14	μs	
Non-dispersive delay from input to one of the outputs <sup>5</sup>	t <sub>O</sub>	f <sub>0</sub>	700	750	800	760	ns	
Non-disp. delay diff. $\tau$ between outputs <sup>6</sup>		f <sub>0</sub>	-	10	60	13	ns	
Number of delay lines on one substrate	_	-	-	2	_	2	_	
Number of input ports	_	_	_	1	_	1	_	
Number of output ports	-	-	_	2	_	2	-	
Group delay for <sup>7</sup> delay line 1	<sup>τ</sup> g1(f)	_	_	t <sub>0</sub> -K <sub>d</sub> (f-f <sub>0</sub> )	_	_	μs	
Group delay for <sup>8</sup> delay line 2			_	t <sub>0+</sub> K <sub>d</sub> (f-f <sub>0</sub> )	_	_	μs	
Operating temperature range	Τ <sub>0</sub>	_	-40	20	85	22	°C	

#### Table 3: Measurement results



Parameter	Symbol	Conditions	Min	Typical	Max	Measured	Unit
Difference in average insertion loss between both lines	-	at f <sub>0</sub> , T <sub>0</sub> =20°C	_	<3	_	1.3	dB
Average <sup>9</sup> VSWR input	VSWR <sub>in</sub>	R <sub>0</sub> ,T <sub>0</sub>	_	20	40	20.19	_
Average <sup>10</sup> VSWR output	VSWR <sub>out</sub>	R <sub>0</sub> ,T <sub>0</sub>	_	30	50	27.92	_
Source and load impedance	R <sub>0</sub>	-	_	50	_	50	Ω
Dimension of the chip	-	_	_	1.2 x 6.5	_	1.2 x 6.5	mm <sup>2</sup>
Dimensions of the hous- ing	_	_	_	6.5 x 13.3	_	6.5 x 13.3	mm <sup>2</sup>

#### Table 3: Measurement results

1. The center frequency of the CDDL is the common center frequency of both test signals (up-chirp and downchirp) for which the run time difference of the compressed pulses is equal.

2. The averaging is done over the signal bandwidth from 210 to 290 MHz.

3. Referred to average insertion loss.

4. The gradient of dispersion includes always Fresnel ripples; therefore, the average (linear interpolation) is decisive.

5. Delay of a compressed pulse relative to the center position of the incoming chirp signal. This parameter is most sensitive against changes of temperature. Therefore a large range is specified.

6. See footnote 5.

7. This is most important to distinguish between the respective output ports of the 3 ports in Figure 1: < Emphasis Footnote>"Complementary Dispersive Delay Line schematic" on page 1–1.

8. See footnote 7.

9. The averaging is done over the signal bandwidth from 210 to 290 MHz.

10. See footnote 9.



# 4 Absolute Maximum Ratings

Parameter	Value	Units
Maximum RF power applied	20	dBm
Temperatures		
Operating temperature (operating ambient temperature range)	+85	°C
Storage temperature (storage temperature range)	+125	°C
Reflow solder temperature (lead-free package)	242	°C

Table 1: Absolute maximum ratings



It is critical that the ratings provided in *Absolute Maximum Ratings* on page 8 be carefully observed. Stress exceeding one or more of these limiting values may cause permanent damage to the device.

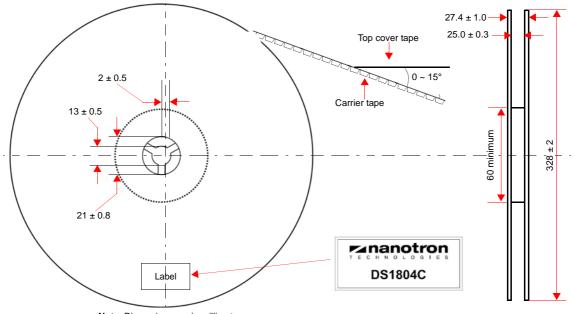


# 5 Tape and Reel Information

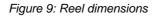
An embossed tape and reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for the CDDL and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the peel-back cover tape.

### 5.1 Reel Dimensions

- Reel diameter: 13 inches (328 ± 2 mm)
- Hub diameter: 5 inches (13 mm)
- Units per reel: 2,500



Note: Dimensions are in millimeters.



### 5.2 Tape Dimensions

#### 5.2.1 Tape Specifications

- 1. Tensile strength of carrier tape: 4.4N/mm width
- 2. Top cover tape adhesion:
  - Pull off angle: 0~15°
  - Speed: 300 mm / minute
  - Force: 20~70g





### 5.2.2 Tape Running Direction

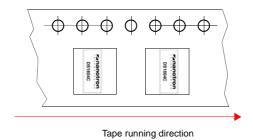


Figure 10: Tape running direction

#### 5.2.3 Leader Part and Vacant Position Specifications

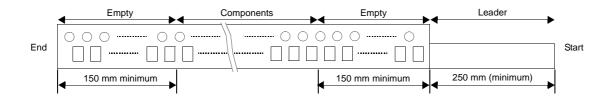


Figure 11: Tape leader and vacant positions specifications

### 5.2.4 Tape Dimensions

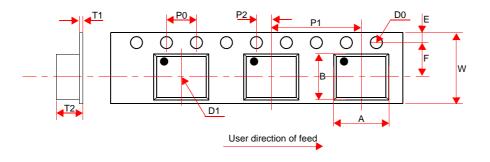


Figure 12: Tape dimensions

Table 4	1: Legena	l - tape di	imension	s (in millii	neters)	

w	F	E	P0	P1	P2	D0	D1	T1	T2	А	В
24.0	11.5	1.75	4.0	12.0	2.0	Φ1.5	Φ1.5	0.3	1.8	6.7	13.6
±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.25	±0.05	±0.1	±0.1	±0.1



# 6 Ordering Information

To order the product described in this document, use the following information.

Part Number	Package Type	Package Quantity	RoHS Compliant
DS1804C	Tape and reel	2,500 pieces per tape	Yes. A certificate of RoHS compliance is available from Nan- otron Technologies on request.

Table 2: Ordering information





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# **Revision History**

Version	Date	Description/Changes
2.00	2004-04-07	Picture of test board added Target specification copied from document NA-02-0143-0135-1.00 Measurement data copied from document NA-03-0143-0216-1.00 Specified data from VSWR input and output exchanged the type.and measured size of die and package are now equal temperature range changed from -20+70 to the values of TRX chip -4085 Center frequency changed: Date of copy right actualized to 2004 Numbering of figures added back ground printing "confidential & preliminary" removed Filter size in scale 10:1 Pad landing in scale 10:1 Pad landing area for pin 1 increased
3.00	2004-04-26	Changes in simulation of gradient of dispersion. The notation of the pins is changed. At all ports the P and N part is exchanged, to be compatible with current board layout nanoNET_TRX_module_V5.brd.
4.00	2004-05-13	Additional chapter for average insertion loss. New value for av. insert. loss in table. Last sentence in chapter 4.4 changed
4.01	2004-07-20	Package dimensions added.
4.02	TBD	Document template updated. Absolute maximum ratings added; packing infor- mation added; ordering information added; CDDL notation standardized; minor textual changes; company address updated.
5.00	2007-08-21	Minor Corrections to text and graphics. Minor editing throughout.



# About Nanotron Technologies GmbH

*Nanotron Technologies GmbH* develops world-class wireless products for demanding applications based on its patented Chirp transmission system - an innovation that guarantees high robustness, optimal use of the available bandwidth, and low energy consumption. Since the beginning of 2005, Nanotron's Chirp technology has been a part of the IEEE 802.15.4a draft standard for wireless PANs which require extremely robust communication and low power consumption.

ICs and RF modules include *nanoNET TRX Transceiver*, *nanoLOC TRX Transceiver*, and ready-to-use or custom wireless solutions. These include, but are not limited to, industrial monitoring and control applications, medical applications (Active RFID), security applications, and Real Time Location Systems (RTLS). *nanoNET* is certified in Europe, United States, and Japan and supplied to customers worldwide.

Headquartered in Berlin, Germany, *Nanotron Technologies GmbH* was founded in 1991 and is an active member of IEEE and the ZigBee alliance.

#### **Further Information**

For more information about this product and other products from Nanotron Technologies, contact a sales representative at the following address:

Nanotron Technologies GmbH Alt-Moabit 60 10555 Berlin, Germany Phone: +49 30 399 954 - 0 Fax: +49 30 399 954 - 188 Email: sales@nanotron.com Internet: www.nanotron.com