

UNG_8266_EVB-LAN9254-DIGIO

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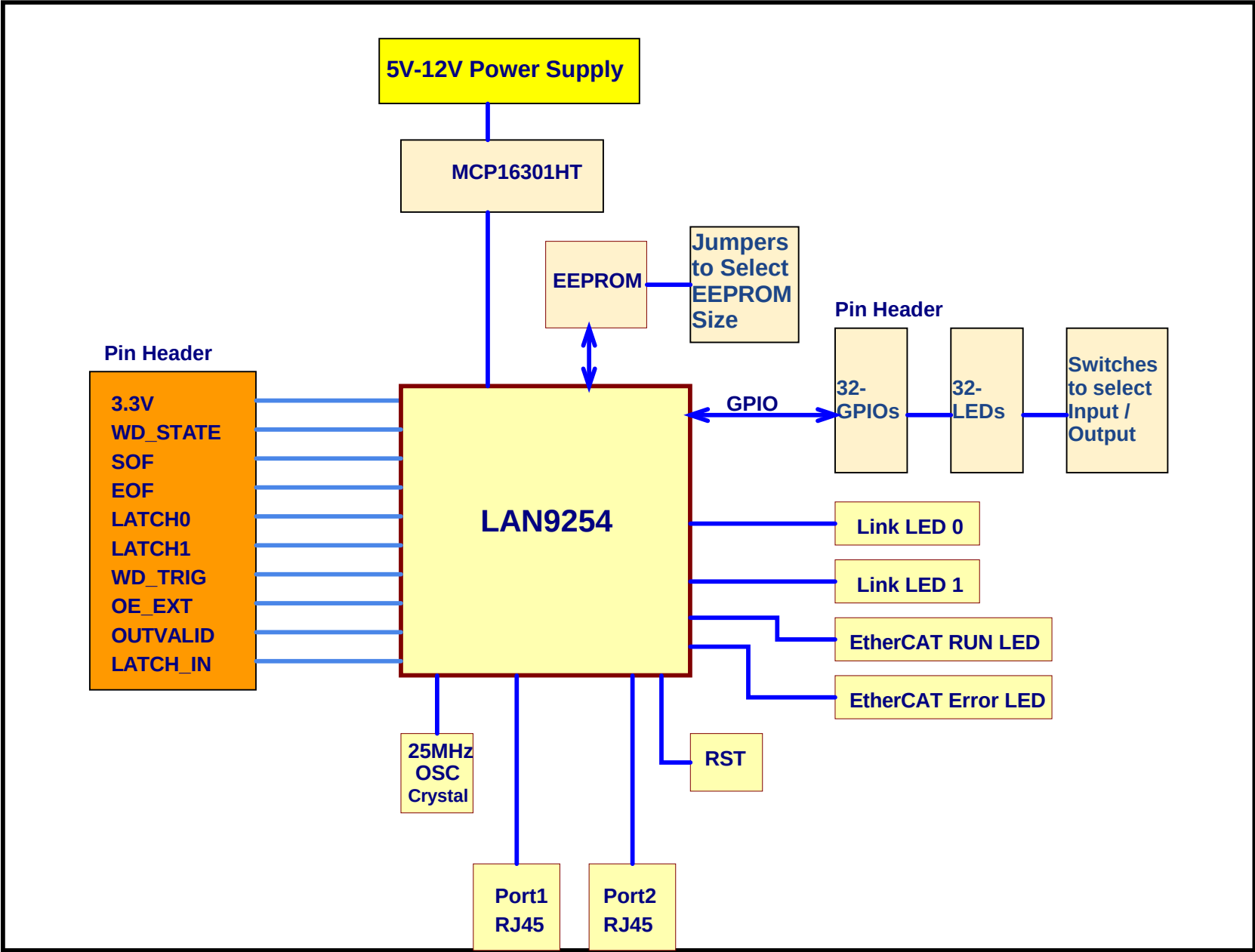
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Revision History

Rev.	Date	Revision Summary	Author
A00	04 20 2020	Initial Version	Xuelu Li

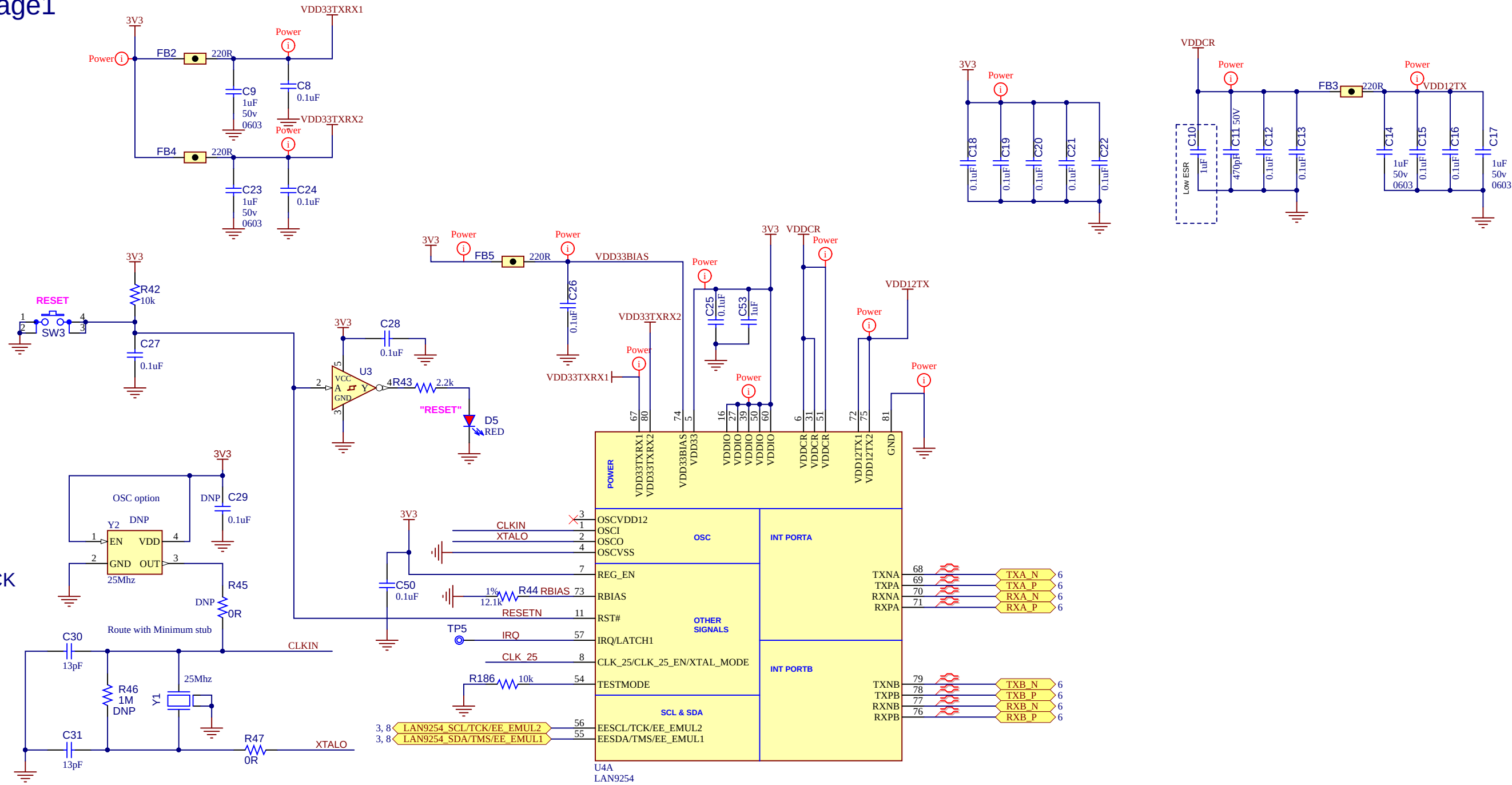
Block Diagram

EVB-LAN9254-DIGIO
Block Diagram

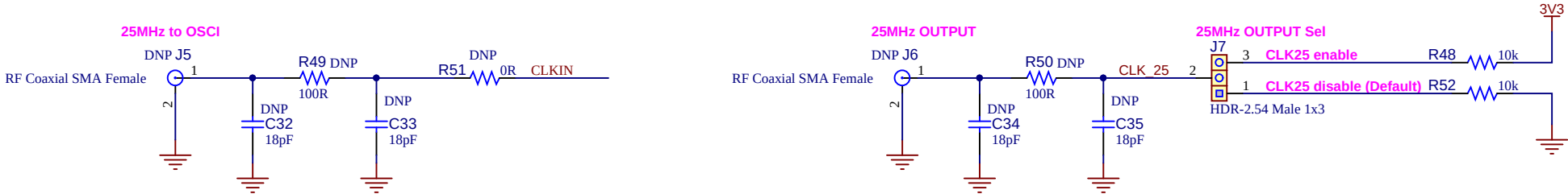


MICROCHIP		Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com		Designed with Altium.com	
Description: LAN9254 Evaluation Board					
Page Title: Power supply & I2C					
Project Name: EVb-LAN9254-DIGIO				PN: EVb-LAN9254-DIGIO	
Size: B	Date: 6/22/2020	Designer: Xuelu Li		Sheet 3 of 8	Rev A0

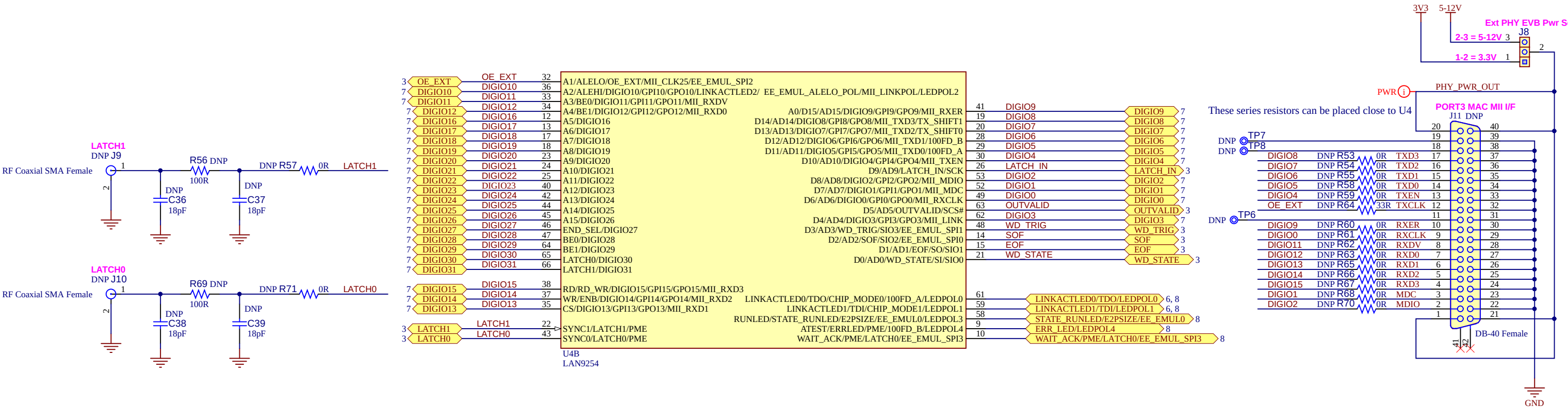
LAN9254-Page1



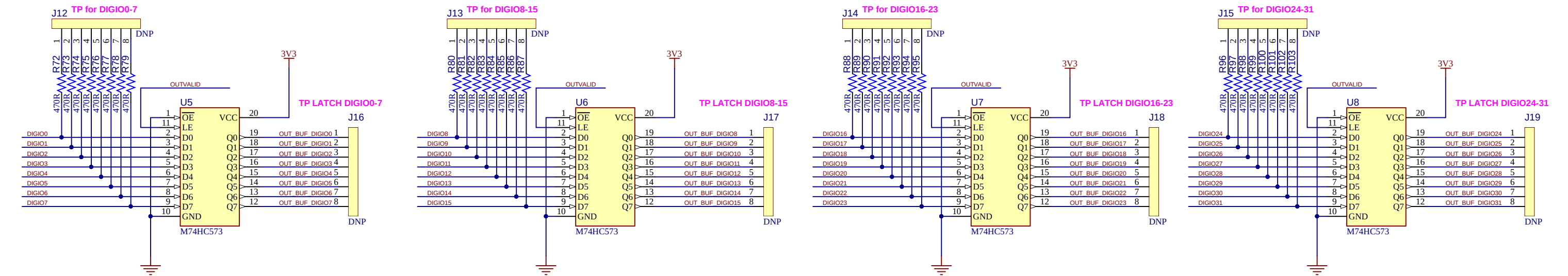
Only external 25MHz crystal is assembled



LAN9254-Page2, buffer Latch and MII Connector



DIGITAL I/O BUFFER



Substitute BOM parts	J12-1	J13-1	J14-1	J15-1
HDR-2.54 Male 2x8	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

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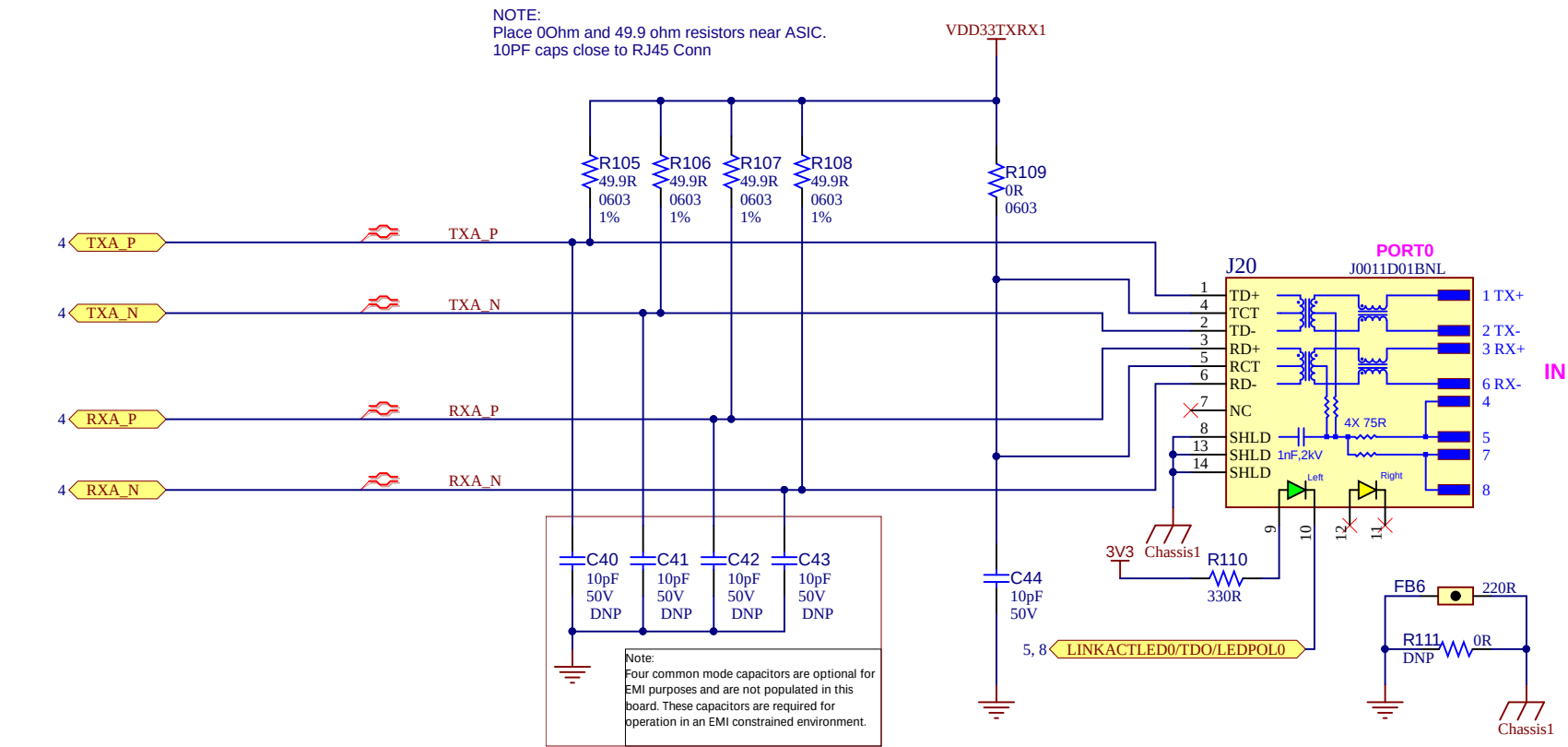
Description: **LAN9254 Evaluation Board**

Page Title: **LAN9254-Page2**

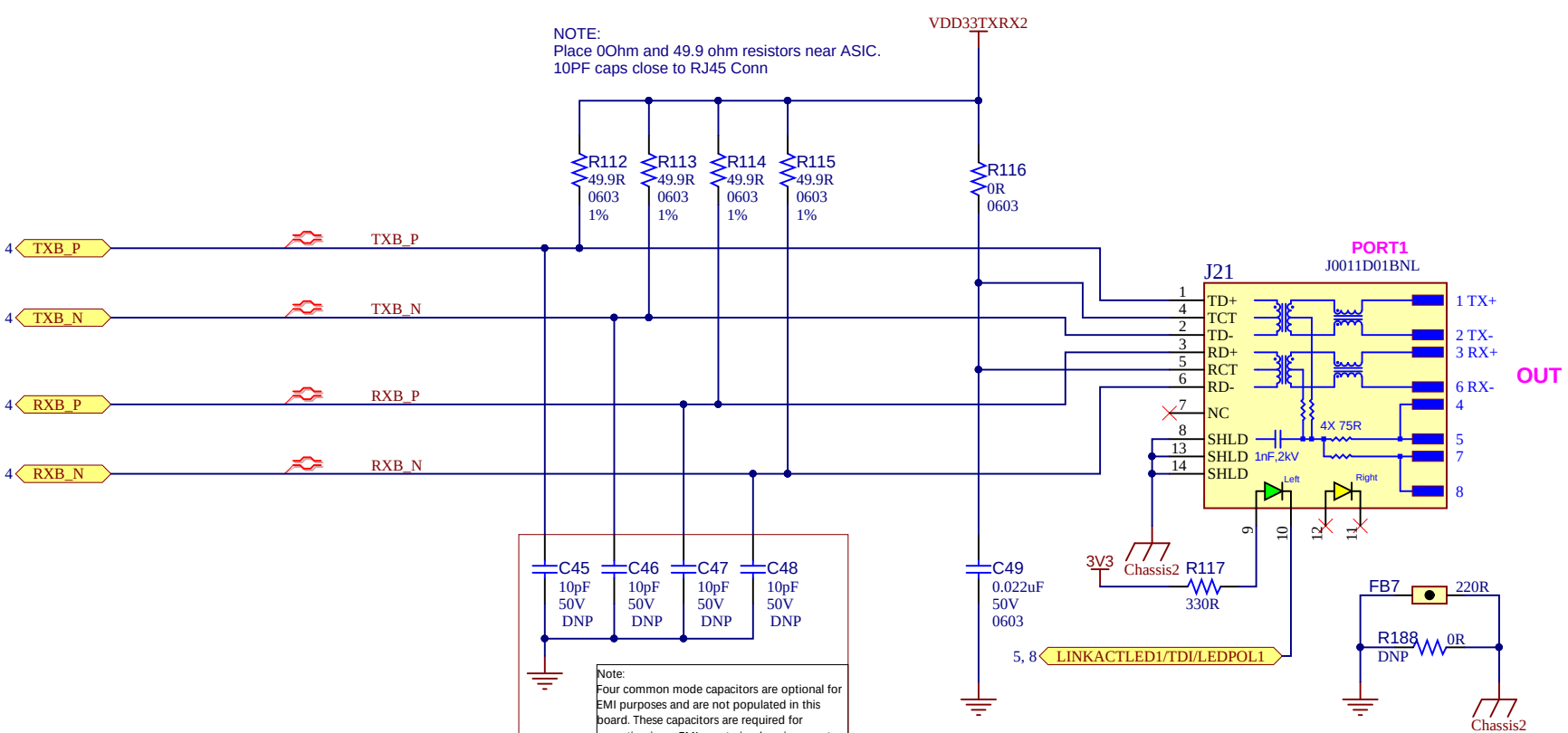
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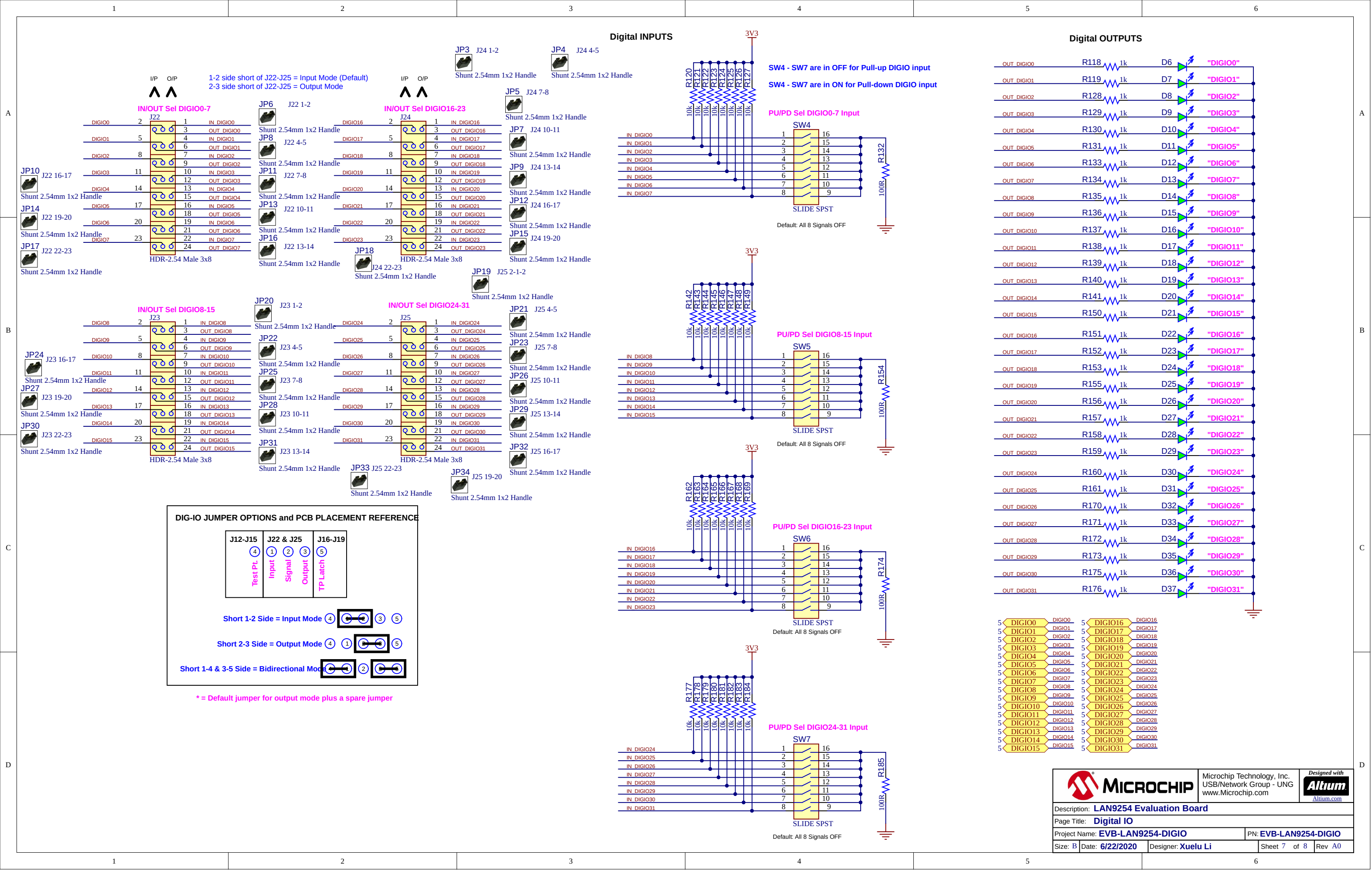
Size: B Date: **6/22/2020** Designer: **Xuelu Li** Sheet 5 of 8 Rev A0

Port0 (IN)

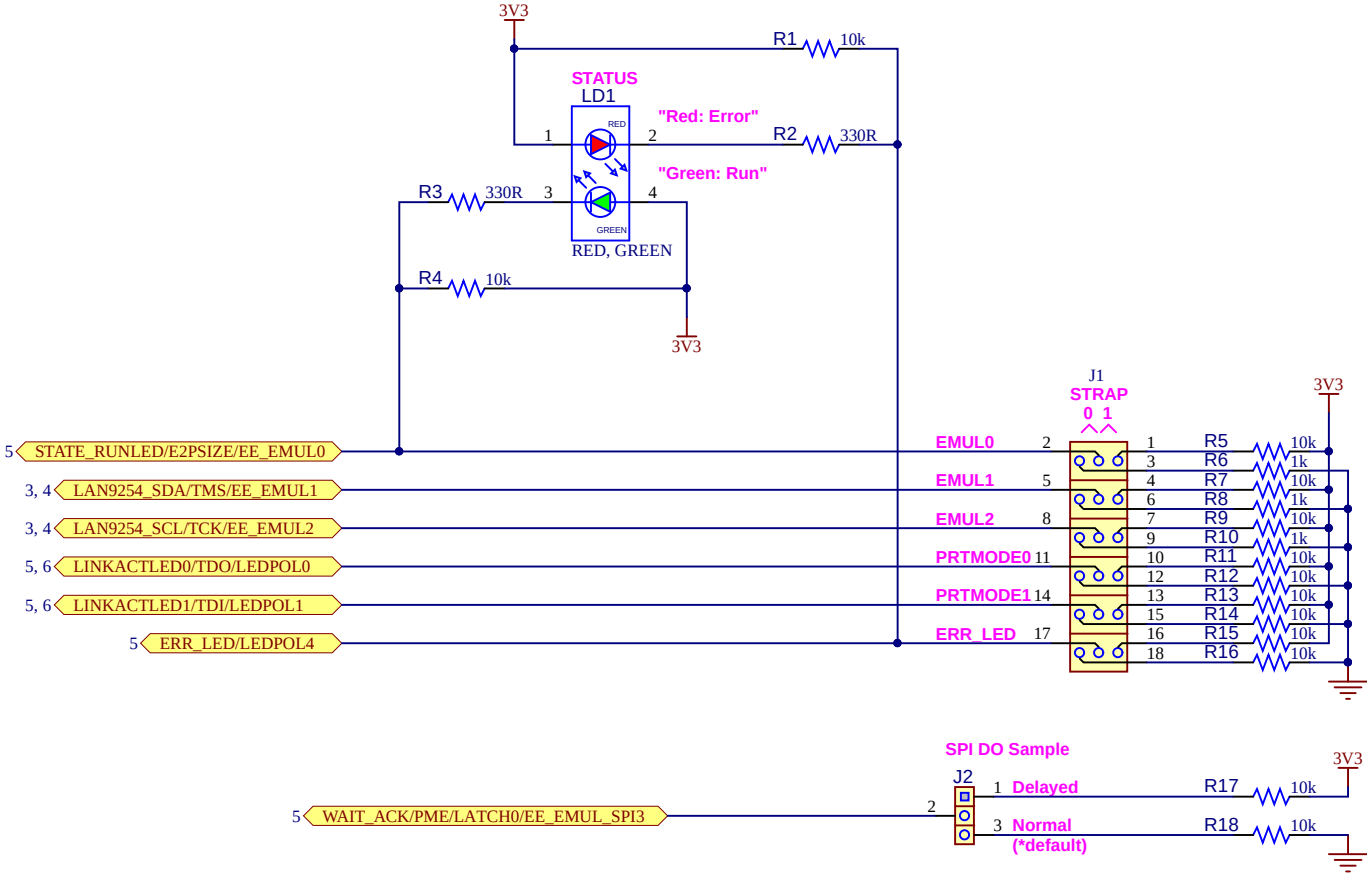


Port1 (OUT)





LED and Strapping



EE_EMUL[2,1,0] (J1[7 8 9, 4 5 6, 1 2 3]), 1-2 side close=1, 2-3 side close=0
000: SPI Indirect Mode
001: HBI Demultiplexed 16-bit EtherCAT Direct Mapped.
010: HBI Multiplexed 1 Phase 16-bit EtherCAT Direct Mapped
011: HBI Multiplexed 2 Phase 16-bit EtherCAT Direct Mapped
100: SPI EtherCAT Direct Mapped
101: Beckoff SPI Mode
110: N/A EEPROM is enabled)
111: N/A EEPROM is enabled)

PRTMODE[1,0] (J1[13 14 15, 10 11 12]), 1-2 side close=1, 2-3 side close=0
0X: 2-Port mode, Port 0 and port 1 are connected to internal PHYs A and B.
10: 3-Port downstream mode, Port 0 and port 1 are connected to internal PHYs A and B, Port 2 is connected to the external MII pins.
11: 3-Port upstream mode, Port 2 and port 1 are connected to internal PHYs A and B, Port 0 is connected to the external MII pins.

J1[(16,17,18), 1-2 side close=1, 2-3 side close=0
ERR_LED Indication, (17-18 default)

J2
2-3 Close: Normal Data Out sample (Default)
(SPI_SO and SPI_SI are sample at same SPI_CLK edges)
1-2 Close: Later Data Out sample
(SPI_SO and SPI_SI are sample at different SPI_CLK edges)

