PSpice Libraries for OptiMOS-T n-Channel Power Transistors

The Simulation Model is subject to change without notice. In addition, models can be a useful tool in evaluating device performance, they cannot reflect the accurate device performance under all conditions, nor are they intended to replace bread boarding for final verification. Infineon therefore does not assume any warranty or liability whatsoever arising from their use. Infineon does not assume any warranty or liability for the values and functions of the Simulation Model.

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Models provided by Infineon are not warranted by Infineon as completely and comprehensively representing all the specifications and operating characteristics of the semiconductor products to which these models relate. The models describe the characteristics of typical devices. In all cases, the current data sheet information for a given device is the conclusive design guideline and the only actual performance specification.

1 Installation

The downloaded modelling package consists of the following files relevant to the PSpice simulator:

- ***.lib file(s) comprising the PSpice code
- ***.slb file(s) providing symbols for the models required by the graphic user interface (GUI) 'Schematics'. (In order to be usable in evaluation versions of the PSpice/Schematics system, each symbol library does not contain more than twenty symbols.)
- ***.olb file(s) comprising symbols for the graphical user interface 'Capture'

If 'Schematics' is used as GUI, the ***.lib files must be installed via the 'Analysis → Library and Include Files' menu. Permanent installation via 'Add Library*' is recommended. The ***.slb files need to be installed via the menu 'Options → Editor Configuration → Library Settings'.

The installation in 'Capture' is similar. The ***.lib files must be included via the 'PSpice → Edit (New) Simulation Profile → Libraries' menu. Using the 'Add as Global' button will provide the device models permanently. The symbol libraries (***.olb files) need to be included via 'Place → Part → Add Library'.

2 Infineon's Modelling Levels

Infineon provides different types of models for MOSFET devices. Level 1 and level 3 types are based on a physical temperature-dependent model of the OptiMOS-T structure and the package.

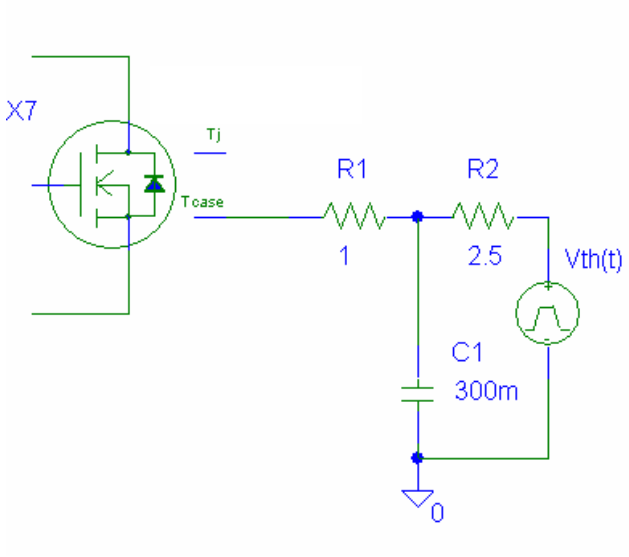

Fig. 1 Connecting a heat sink model to the device model

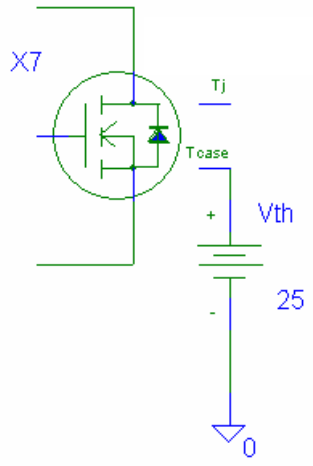

Fig. 2 Modelling of an ideal heat sink

Level 1 models assume a constant device temperature for the entire circuit and during a transient simulation (the temperature is to be given in the Analysis Setup)

In order to be able to compute the self-heating dynamically, the electrical model is coupled with a thermal model of the device in Level 3 models. To do this, the current power dissipation in the transistor is determined permanently, and a current proportional to this power is fed into the thermal equivalent network. The voltage at the Tj node then contains the information about the time-dependent junction temperature which in turn acts directly on the temperature-dependent electrical model.

Level 3 models of single devices (one chip per package) have two external thermal nodes: First, there is Tj, where the user can monitor the junction temperature easily. Usually, this node should not be connected. However, when the computation should start with a device junction temperature different to the thermal equilibrium, connecting Tj with a small capacitor (typically 1pF) to ground and stating an initial value (parameter IC) for the initial potential difference (which is used as a measure for the initial temperature in °C) enables these types of simulations. The second thermal pin is Tcase (in TO packages), Tsolder_joint (in small signal packages like SO, SOT) or Tpad (in die models). This pin has to be connected. An external resistor-capacitor-network can be added between the Tcase pin and ground. The right-hand-side terminal of the heatsink RC-network has to be connected to a voltage source which represents the ambient temperature (Fig. 1). On the other hand, connecting the ambient temperature source directly to the Tcase pin leads to a network where optimum heat transfer is modelled (Fig. 2).

Level 3 models for dual devices (ie devices comprising two dice) have a coupled thermal network which allows to compute the temperature rise in both chips for any switching state. Typically, these models have two pins for the junction temperatures (Tj1, Tj2) and the pins Tsolder_joint1 and Tsolder_joint2. Since often the thermal coupling between the two MOSFET subsystems is not restricted to internal heat flow, the external RC-networks should be connected in these cases as well. For example, if the drain pins of both MOSFETs are connected electrically directly at the device, the external coupling is

considerable and, as a good approximation, the thermal pins Tsolder_joint1 and Tsolder_joint2 can be shorted (Fig. 3).

The part names of Level 3 models are similar to the device names. For example, the Level 3 model of the IPP25N06S3-25 has the part name IPP25N06S3-25. Level 1 models can be accessed using the suffix L1, respectively. Hence, the model of the product above is named IPP25N06S3-25_L1.

If the simulation focus is more on speed and not on accuracy, also simplified models are provided. These models can also be used in other Spice-type simulators that do not work with PSpice-specific syntax like function statements. The model name of the IPP25N06S3-25 would be IPP25N06S3_25, ie an underscore is used.

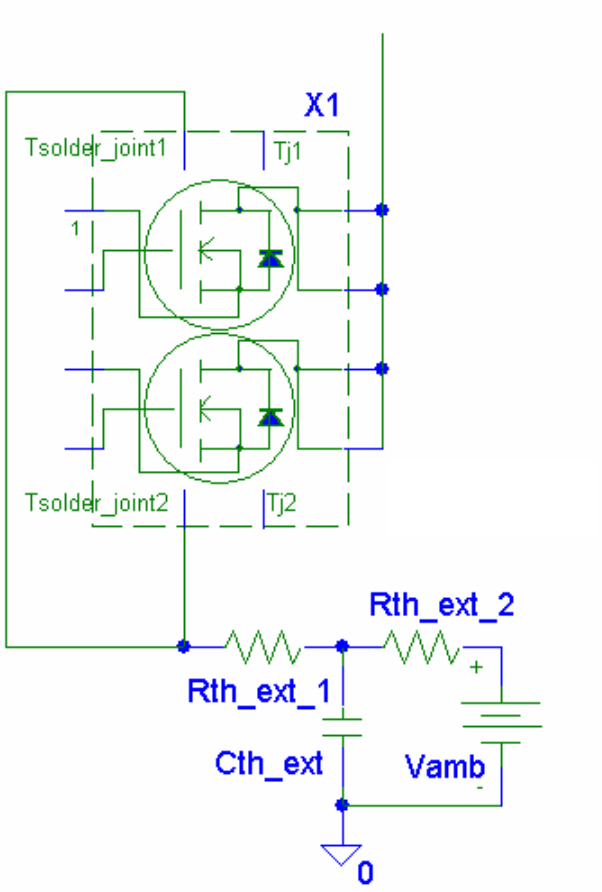

Fig. 3 Ideal external thermal coupling of the dice of a dual device. Rth_ext_1/2 and Cth_ext model the heat sink.

3 Underlying Structure of the Models

Sometimes it is helpful to have knowledge of the potentials and currents within the device. In order to be able to pick the correct nodes, Fig. 4 provides the basic structure of the Level 3 system of a single OptiMOS-T n-channel device.

The models take account of the behaviour of the parasitics of the MOSFET device. For example, the ohmic and inductive characteristics of the package are modelled. To include these and other features, additional active and passive components are necessary. Since the internal structure of most of these components (especially on the chip modelling level) is not important for the user, simplified structures are shown in the graphics.

As the parasitic inductances of the devices depend strongly on the layout of the board, default values of the source, gate and drain parasitic inductances are set to estimated values and can be changed by the user. Proper values for other layouts can be found by analysing the ringing frequencies of measured wave forms. As an example: We found values of 2-3 nH total parasitic inductance for a buck converter evaluation board using SO-8 devices and around 10 nH for a D^2Pak solution on a motherboard. These values have to be split up into the drain and source inductances of the control and syncronous FET.

Dual devices have a similar topology. However, internal nodes have the additional letter ‘a’ or ‘b’ as suffix, whereas external nodes have numbers (1 or 2) to be distinguishable. The thermal network for these cases depends on the package type and has therefore variable node names.

As an example, to evaluate the heat dissipation in the chip, the current through `X1.G_TH` can be monitored if a Level 3 model is used.

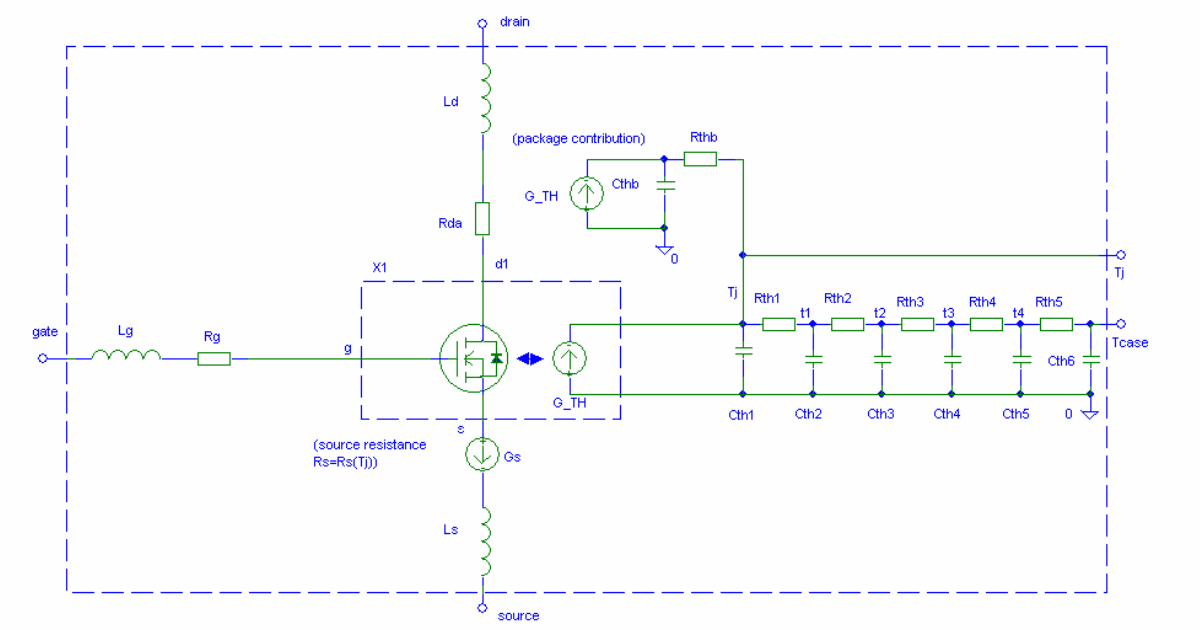

Fig. 4: Underlying model structure of a packaged Level 3 OptiMOS-T n-channel device

4 Optional Parameters for OptiMOS-T Models

OptiMOS-T model parameters are chosen to give the behaviour of a typical device. However, in order to enable worst-case and sensitivity analyses, OptiMOS-T models provide several important parameters to the user.

Generally, the deviations are scaled to the range [-1;1] where a value of –1 refers to the minimum value, 0 is the typical value (default) and 1 accounts for the maximum value of the model parameter. Note that the parameters have different priorities, such that not all combinations are possible.

Variations of the transconductance are modelled with the parameter `dgfs` which has a range of [-1;0].

The next parameter is `dRdson`, which enables the user to consider the maximum on-state resistance of the device. The allowed range is [0;1]. If `dRdson`≠0, entries in `dgfs` are overwritten.

Models have the attribute dVth to model threshold voltage deviations from the typical value. The allowed range is [-1;1]. If dVth≠0, entries in dgfs and dRdson are set to zero.

Variations in the capacitances are considered by assigning a value to dC, where values in the range [0;1] are possible.

Furthermore, level 3 models also have the parameter dZth, where values in the range [0;1] are allowed to vary between typical and guaranteed thermal performance.

The parameters of dual devices are accessible individually and named dVth1, dVth2, dgfs1, dgf2, etc.

The modelling of device performance deviations is a complex task since typically there is no one-to-one relation between a deviation in the manufacturing process and the variation in a particular device parameter. The use of the given optional parameters does therefore not account for all cases and might in special cases even result in performance that does not fulfil the specifications guaranteed by Infineon.

Further parameters are the source inductance Ls, the drain inductance Ld and the gate inductance Lg. The default values are set to extracted values from measurements. Sensible values are between 0 (for a ideally designed layout) and around 10 nH (poorly designed layout). See section 3 for further hints.

5 Typical Simulation Parameters

As PSpice was originally not designed for power electronics and highly non-linear components, the standard simulation parameters (Simulation Setup/Options) are often not suitable. If great currents occur in the circuit, commonly the following typical values facilitate convergence:

ABSTOL=	10pA..10nA	(maximum current accuracy)
CHGTOL=	0.01pC..1pC	(maximum charge accuracy)
ITL1=	150	(maximum number of iterations for DC analyses without initial conditions)
ITL2=	150	(maximum number of iterations for DC analyses with initial conditions)
ITL4=	50..500	(maximum number of iterations for transient analyses time steps)
RELTOL=	0.01	(relative accuracy of voltages and currents)

In many cases it is necessary to limit the step size for transient analyses. The circuit system contains many different time scales, where the automatic step control of the PSpice simulator sometimes disregards essential fast-time-scale information which eventually leads to convergence problems.

In cases where the time to be simulated (TSTOP) is relatively large (typically if thermal phenomena are of main interest) and sharp gradients are occurring, the minimum step size might be too large. In that cases it is helpful to start with a reduced TSTOP, interrupt the simulation process and change TSTOP to the desired value.